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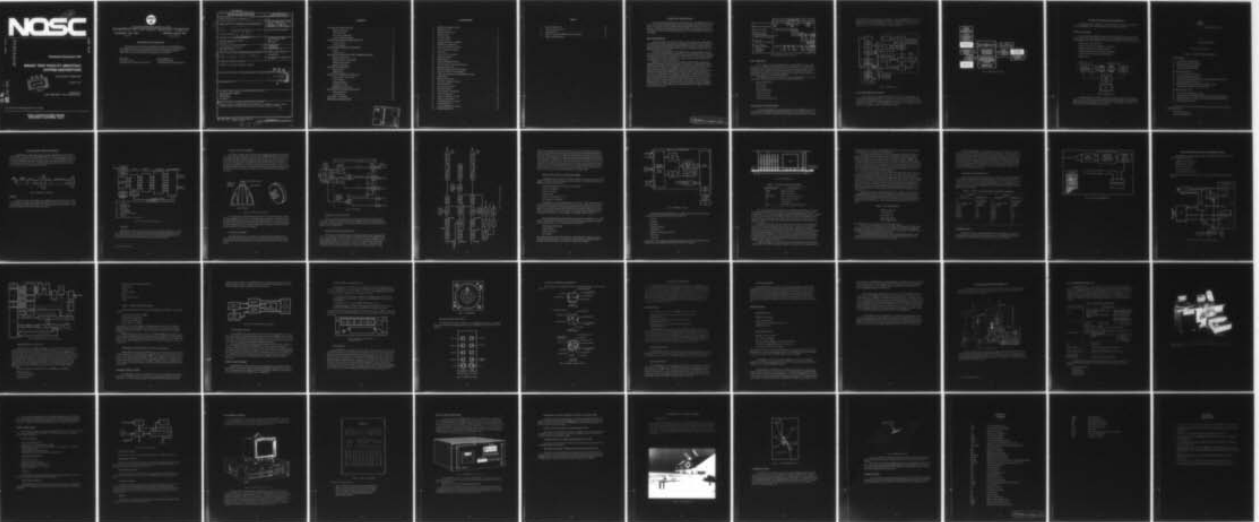
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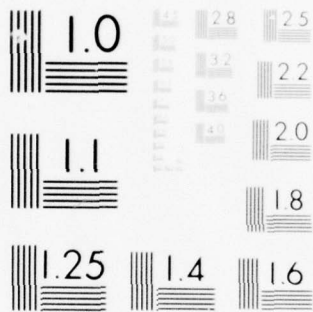
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## Technical Document 104

# BRAZO TEST FACILITY (BRATFAC) SYSTEM DESCRIPTION

JK Hall and LK Sherman

11 March 1977

Prepared for  
USAF ARMAMENT TEST LABORATORY



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Work discussed in this report was performed by members of the Surveillance and Countermeasures Division, Electromagnetic Systems Department for the USAF Armament Test Laboratory under program element 63601F, task area O, and Work Unit AFS (NELC H105). This report was approved for publication 11 March 1977.

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REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER NOSC Technical Document 104 (TD 104) ✓	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER (9)
4. TITLE (and Subtitle) BRAZO TEST FACILITY (BRATFAC) SYSTEM DESCRIPTION.	5. TYPE OF REPORT & PERIOD COVERED Research and Development <i>repts</i> July 1976 - February 1977	
6. PERFORMING ORG. REPORT NUMBER		7. AUTHOR(s) J. K. / Hall JK Hall, LK Sherman L. K. / Sherman
8. CONTRACT OR GRANT NUMBER(s)		9. PERFORMING ORGANIZATION NAME AND ADDRESS Naval Ocean Systems Center (NOSC) ✓ San Diego, CA 92152
10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 63601F; 0; AFS NELC H105		11. CONTROLLING OFFICE NAME AND ADDRESS USAF Armament Test Laboratory Eglin AFB, FL 32542
12. REPORT DATE 11 March 1977		13. NUMBER OF PAGES 54
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office) NOSC/TD-104 (12) 53p.		15. SECURITY CLASS. (of this report) UNCLASSIFIED
16. DISTRIBUTION STATEMENT (of this Report) Approved for public release; distribution is unlimited		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)		
18. SUPPLEMENTARY NOTES		
19. KEY WORDS (Continue on reverse side if necessary and identify by block number) Anti-radiation Missile (BRAZO) Homing devices Automatic testing Test facilities		
20. ABSTRACT (Continue on reverse side if necessary and identify by block number) Operational features of the BRAZO missile and test facilities for its evaluation are described. System-integration activities and test-data collection, reduction, and analysis procedures are discussed.		

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## SECTION ONE, INTRODUCTION

This report provides information on operational features of the BRAZO missile and the test facilities which have been developed to test and evaluate the GTU-5 version of this missile. A companion document entitled "BRATFAC Master Test Plan" defines the test program, the required system-integration activities, and the test-data collection, reduction, and analysis procedures which are being implemented to verify the BRAZO weapon-system performance.

### BRAZO BACKGROUND

The Navy and Air Force tactical air missions require air superiority in high-density engagements and in highly sophisticated electromagnetic environments. Passive radar detection, discrimination, and anti-radiation homing (ARH) and guidance techniques provide a significant potential for improvement in US air power as well as denial to the enemy of the free use of airborne radar systems.

The passive homing capability of the BRAZO air-to-air missile provides a weapon which can passively engage hostile aircraft which emit rf energy whether they be surveillance, command control, intercept, or jammer units. Passive guidance provides launch and maneuver capabilities with an inherent potential for use against surface targets whose radiation bands overlap those of the air-target threats.

BRAZO is an outgrowth of the Electromagnetic Radiation Source Elimination (ERASE) program which sponsored the design and development of Anti-Radiation Missile (ARM) sensor technology. The development of technology to support the seeker requirements (eg, radome, antenna, local oscillator, IF processor, and video processor) was approached from the baseline capabilities established in ERASE. Brassboard hardware was fabricated and designed as the Mod 0 seeker. Laboratory tests, anechoic-chamber tests, sled tests, and captive-flight tests validated the seeker design. Flightworthy seekers were then fabricated and integrated with an AIM-7E-2 airframe and control system. An F-4D aircraft was modified to accept the BRAZO AIM-7E-2 interface wiring and control and display hardware. The Demonstration Test (sled, captive, guidance) was conducted at Holloman AFB, New Mexico. Milestones for the early development activities of BRAZO are shown in figure 1. Following the successful demonstration tests at Holloman, fabrication of GTU-5 was begun.



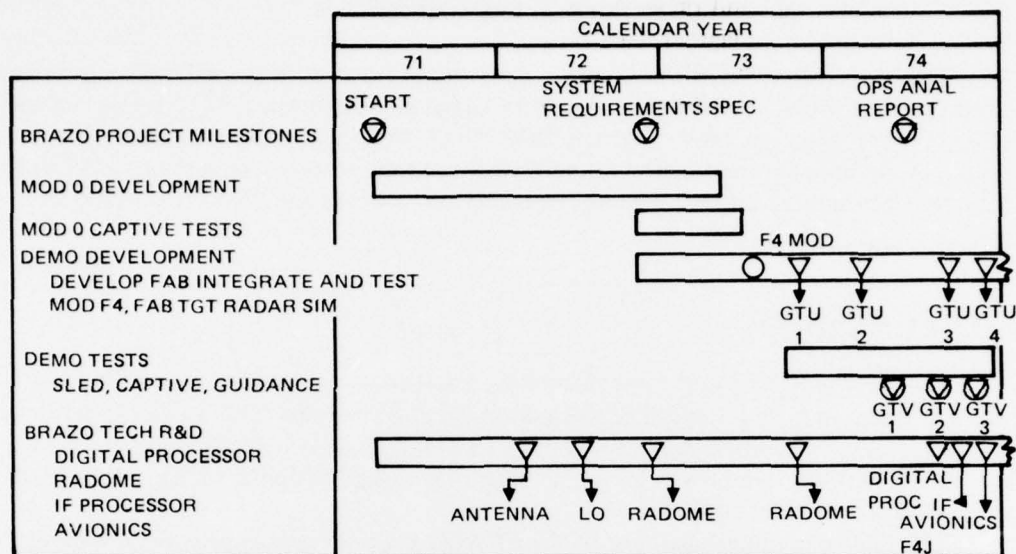


Figure 1. BRAZO demonstration project.

## GTU-5 OBJECTIVES

GTU-5 is being integrated at the BRAZO Test Facility (BRATFAC) with a radar-warning receiver (RWR), and the AERO-1A weapons-control system to comprehensively evaluate the system's ability to passively acquire a target, display and designate the threat, and hand-off to the AERO-1A for acquisition, launch-zone computations, and missile initialization. Data derived from the tests will be utilized to prepare specifications for the Advanced Development Version (ADM) of BRAZO.

GTU-5 implements a digitally controlled version of the analog GTU-1, 2, 3, and 4 models. The following functions were selected for digital implementation:

- Platform stabilization,
- Pulse tracking,
- Threat storage,
- Threat identification,
- Frequency tracking,
- Angle tracking, and
- Steering gain and time-to-go.

## TEST FACILITY CONFIGURATION

A completely integrated test facility will be used to test the BRAZO concept. The major elements of the BRAZO Test Facility (BRATFAC) include an F-4B mounted on a 5-inch gun turret, the GTU-5, BRAZO Avionics Equipment, operational and test software,



instrumentation, test-van, and on-site test facilities. The major BRATFAC system components are shown in block diagram form in figure 2. Although the GTU-5 missile and BRAZO Avionics Equipment (BRAVE) are either brass-board or "off-the-shelf, stand-in" equipments, they are electrically equivalent and fully operational.

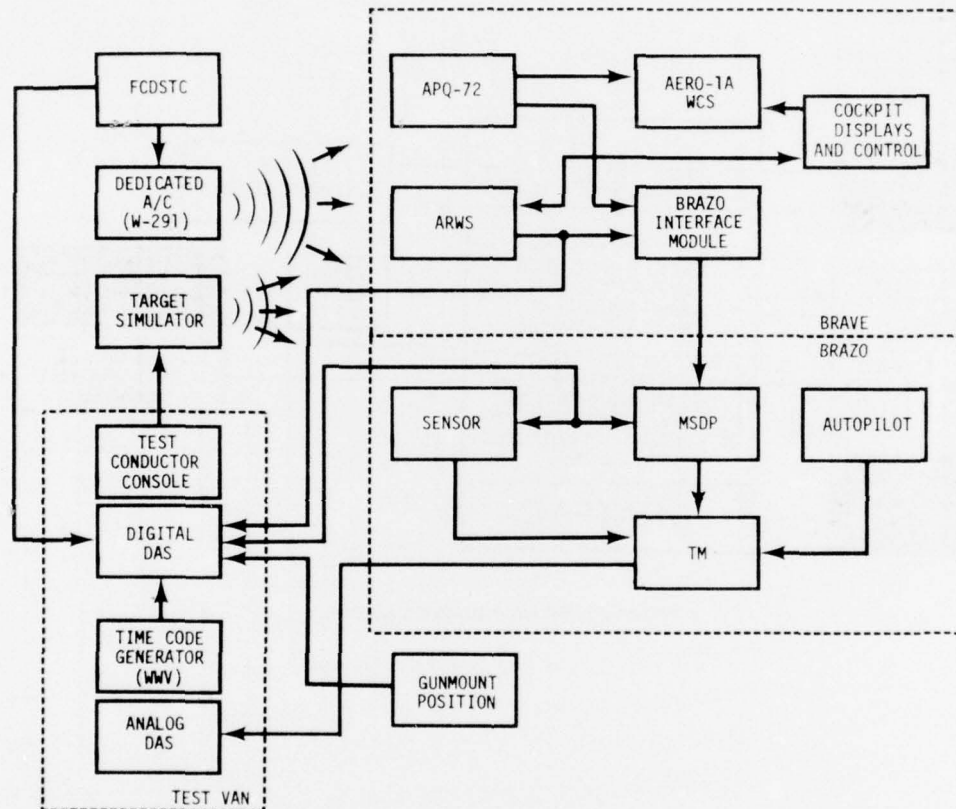


Figure 2. BRATFAC system.

## ADVANCED PROGRAM PLANNING

The GTU-5 test and evaluation program will provide the data/information base for the follow-on BRAZO development and test phases. Subsequent activities which are anticipated for the BRAZO program, including their relation to critical program decisions, are illustrated in figure 3. As shown, BRATFAC is utilized as a self-contained, low-cost facility for evaluating each phase of BRAZO development.



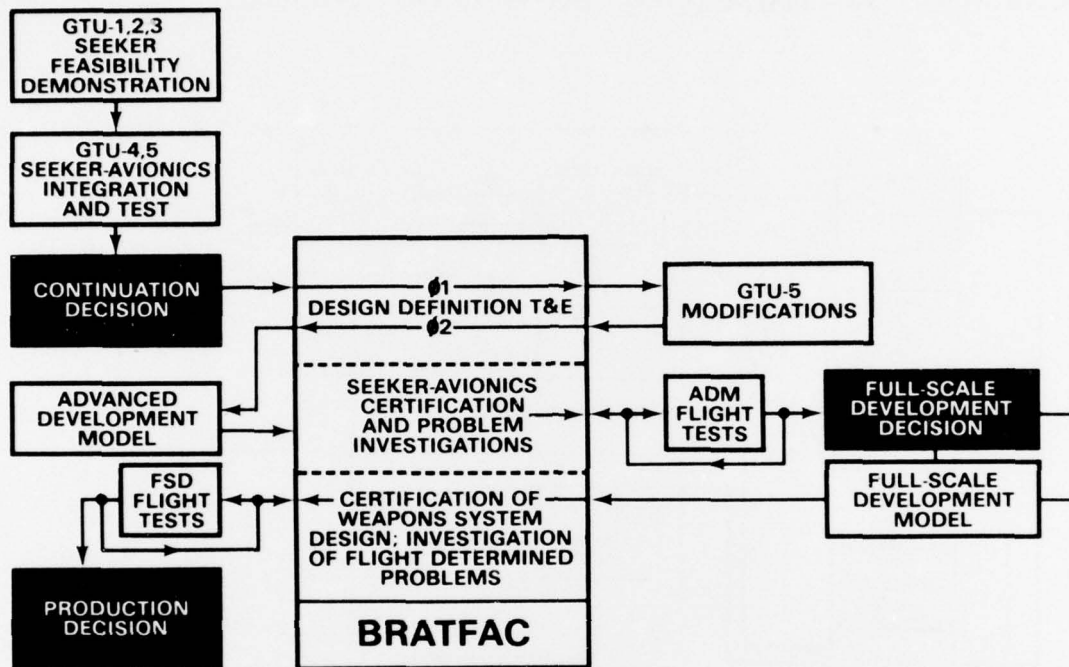


Figure 3. BRAZO program phases.



## SECTION TWO, BRAZO SYSTEM OPERATION

The BRAZO system is designed to attack and destroy enemy airborne targets by detecting, identifying, and tracking the target's electromagnetic emissions.

### TACTICAL FEATURES

Tactical utilization of BRAZO involves the integration of the missile, the aircraft missile-control system, and on-board radar-warning receiver (RWR), and appropriate interface elements (fig 4). The integration of these systems provides these system characteristics:

- Identification of all waveforms,
- Operation in a dense electromagnetic environment,
- Prioritized display and designation of targets,
- Prelaunch target selection and missile initialization,
- Accurate mid-course and terminal homing, and
- Home-on-jam.

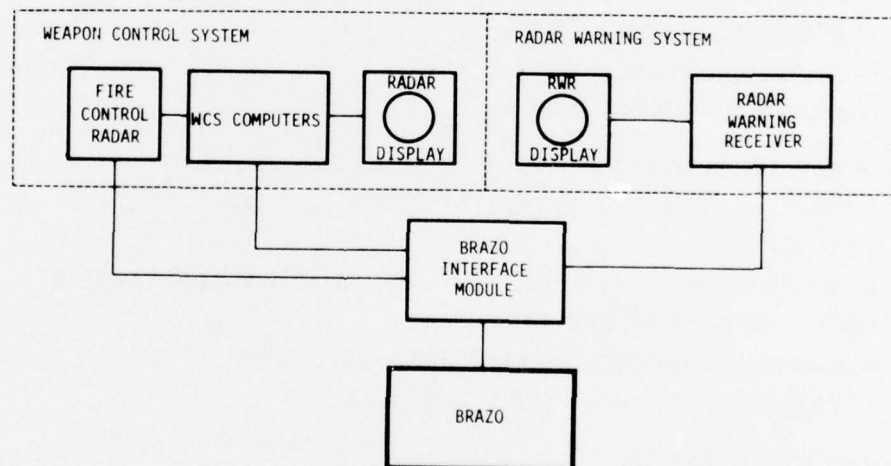


Figure 4. BRAZO system.

The RWR provides the weapon system with an all-aspect ( $360^\circ$ ), detection-range capability. In the critical forward area, the missile seeker significantly extends the RWR range capability as shown in figure 5. Characteristics of the separate systems which comprise the total missile system are shown in table 1.



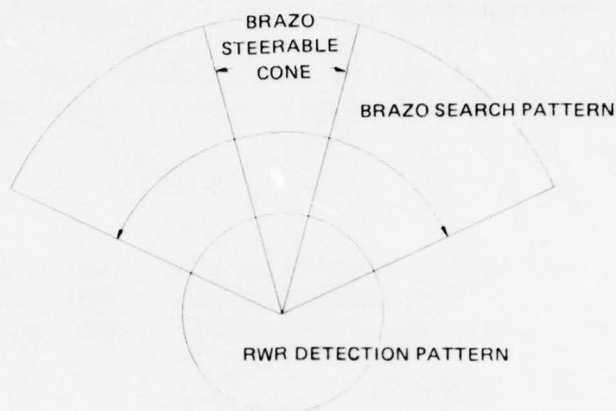


Figure 5. Detection patterns.

TABLE 1. SYSTEMS CHARACTERISTICS.

**BRAZO MISSILE**

- PULSE SORTING AND TRACKING
- THREAT HAND-OFF TO AVIONICS
- GUIDANCE AND STABILIZATION
- POSTLAUNCH MODE CONTROL

**RADAR WARNING SYSTEM**

- 360° LETHAL-THREAT DETECTION
- TURNING COMMANDS TO MISSILE
- CLASSIFICATION AND PRIORITIZATION OF MISSILE-DETECTED TARGETS
- DISPLAY OF PRIORITY TARGETS
- PARAMETERS HAND-OFF TO WEAPON CONTROL SYSTEM
- CORRELATION OF PASSIVE AND ACTIVE DATA

**WEAPON CONTROL SYSTEM**

- ACTIVE TRACK OF PRIORITY TARGET
- LAUNCH ZONES AND STEERING COMMANDS CALCULATION AND DISPLAY
- MISSILE PRELAUNCH FUNCTIONS CALCULATION AND IMPLEMENTATION
- IN-RANGE MISSILE LAUNCH

Several alternative means for determining range-to-target will be examined during BRATFAC testing:

Normal AI radar range,  
AI burst from BRAZO cue,



Tactical data link (air to ground),  
GCI vectoring, and  
Range from wing man.

Other tactical features of BRAZO include its ability to lock on before launch, separate targets in clusters (figure 6) or in a stream, and its capability for all-aspect detection and track (including the minor lobes of enemy emitters). The utilization of BRAZO in a bistatic mode will be evaluated for short-range and dog-fight applications. This mode would be implemented using the aircraft airborne interceptor (AI) radar as an illuminator. Controls and displays are available to the pilot/operator for controlling the modes and functions of the AI radar, the RWR, and the missile, for observing selected targets and launch zones, and for determining range and position of targets.

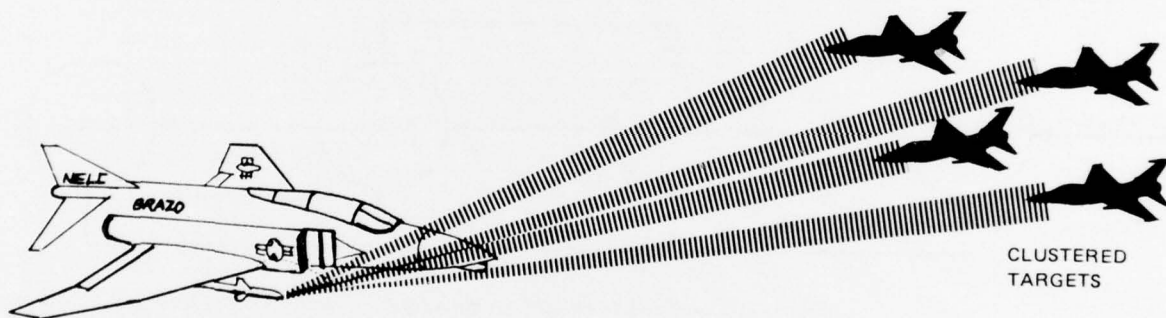


Figure 6. Clustered targets.

## TACTICAL OPERATION

The BRAZO test facility is designed to simulate tactical operating conditions in order to provide a meaningful evaluation of BRAZO performance. What follows is a description of the processes involved in operation at BRATFAC.

The BRAZO system is initiated by the operator depressing the BRAZO button on the Mode Control and Status Unit (MCSU). The system then enters a CLEAR mode in which the Missile Data Processor (MDP) and the advanced radar warning system (ARWS) (subsequently referenced as ATAC/BAP) are initialized. This CLEAR mode must be entered before any other BRAZO function can be performed. CLEAR may be entered from any other system mode to re-initialize the system in the event of a lost target or inability to find a specific target.



After initialization, the operator may then command the system to search for targets. This he does by depressing the SEARCH button on the BRAZO Control Panel (BCP). This causes the system to enter the SEARCH mode. While in this mode, BRAZO searches for targets and the ATAC/BAP displays them by priority to the operator.

The operator may then choose to track a target by depressing the step-reset switch on the MCSU until his chosen target is in the "highest priority" position on the ARWS display tube (CRT). TRACK mode is initiated by depressing the TRACK button on the BCP. The missile then attempts to lock on the highest priority target and notifies the operator when parameter-track lock on is achieved. If lock on cannot be achieved, or if the target is lost, the operator is notified. At this point, ATAC/BAP may choose to again enter the SEARCH mode or the CLEAR mode using the time the lost target was tracked to determine which mode to enter.

After parameter-track lockon, the operator may choose to simulate a launch. LAUNCH mode is commanded by depressing the LAUNCH button on the BCP. When "angle-lock" is achieved, the operator is notified and the missile may be launched or the system may be cleared. A simplified outline of the operational sequence is shown in figure 7. The ATAC/BAP and MDP operations are explained in greater detail in Section 5.

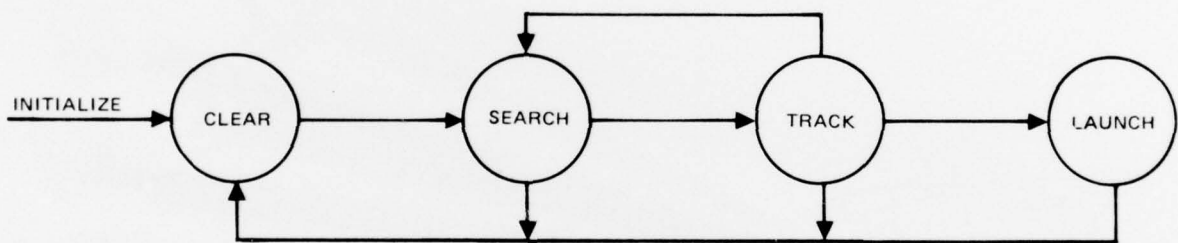


Figure 7. Operational sequence of BRAZO.



### SECTION THREE, MISSILE DESCRIPTION

The BRAZO test configuration consists of a passive anti-radiation homing (ARH) seeker (GTU-5) integrated with a SPARROW (AIM-7E-2) airframe and control system. The passive seeker replaces the original semiactive guidance unit. The SPARROW telemetry unit was adapted to BRAZO requirements and the autopilot was modified and adjusted for electrical compatibility with the seeker. The BRAZO test configuration airframe containing locations of the major subsystems is shown in figure 8.

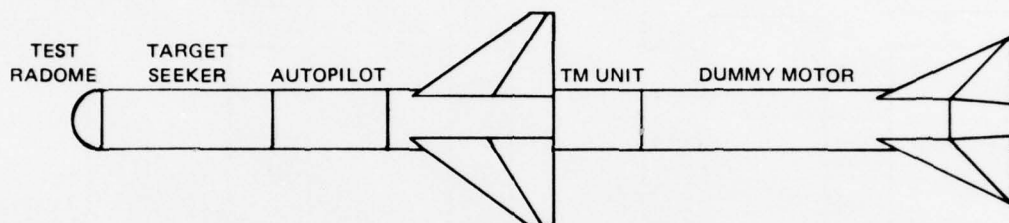


Figure 8. BRAZO test configuration.

#### SEEKER

The Seeker consists of the radome, sensor, digital processor, and electrical conversion unit subsystems. It operates over a multioctave frequency range, detects and processes target radar transmissions, and provides guidance data to the steering section of the missile. A functional block diagram of the seeker is provided in figure 9.



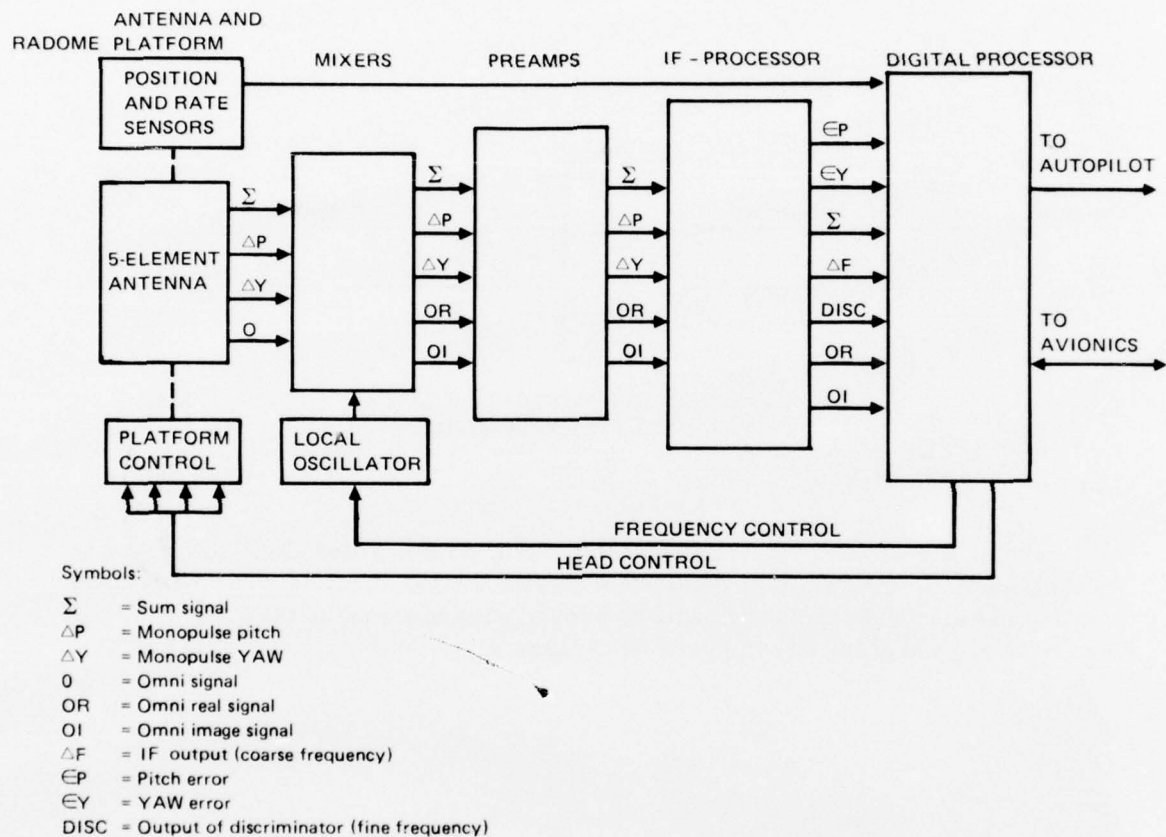


Figure 9. Seeker functional block diagram.

## RADOME

BRATFAC tests will be conducted using an 8-inch hemispherical radome as a "stand-in."\* The performance of this radome was verified in earlier anechoic chamber tests and it was used for numerous captive-flight tests in the F-4D aircraft at Holloman AFB. Its use eliminates the introduction of unpredictable errors into the measurements.

\*1 inch = approx 25.4 mm



## SENSOR ANTENNA ASSEMBLY

The antenna assembly converts the microwave signals to monopulse sum and difference signals. The antenna assembly is mounted on the SPARROW stabilized antenna platform and provides line-of-sight rate signals for missile steering. The antenna consists of four direction-finding (DF) elements positioned as a diamond with a shorter, fifth (omni), element in the center (figure 10). The signals from the four DF elements are combined in a monopulse sum-and-difference network to yield three DF channels ( $\Delta P$ ,  $\Delta Y$  and  $\Sigma$ ). The fifth element provides an input to the omnidirectional channel for sidelobe blanking. It also provides the input to an image-rejection mixer for use in separating the desired signal from the image.

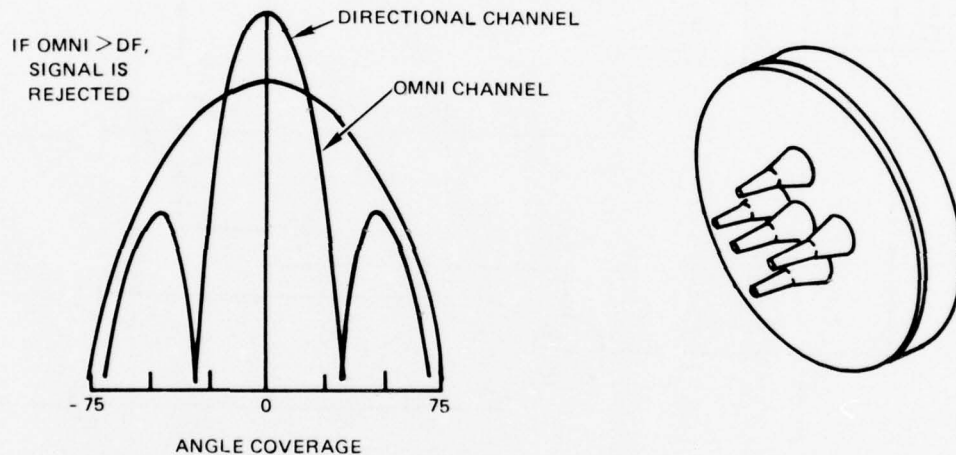


Figure 10. GTU-5 five-element antenna.

The hydraulically controlled gimbal subsystem for the antenna provides an angular positioning capability in both the slave and track modes of operation. The subsystem uses the existing AIM-7E unit, rate gyros, and follow-up potentiometers for feedback to stabilize the head-control subsystem in the track and slave modes, respectively. Output signals from the head-control subsystem are sensor line-of-sight rates used for missile steering, and pitch and yaw positions used to indicate head angles.

## SENSOR RF ASSEMBLY

The rf assembly (figure 11) includes the rf components and the balanced mixers. The mixer system consists of 4 mixers, one in each of the  $\Sigma$ ,  $\Delta P$ , and  $\Delta Y$  channels, which are mounted on the antenna gimbal, and an image-rejection mixer located off the antenna gimbal.



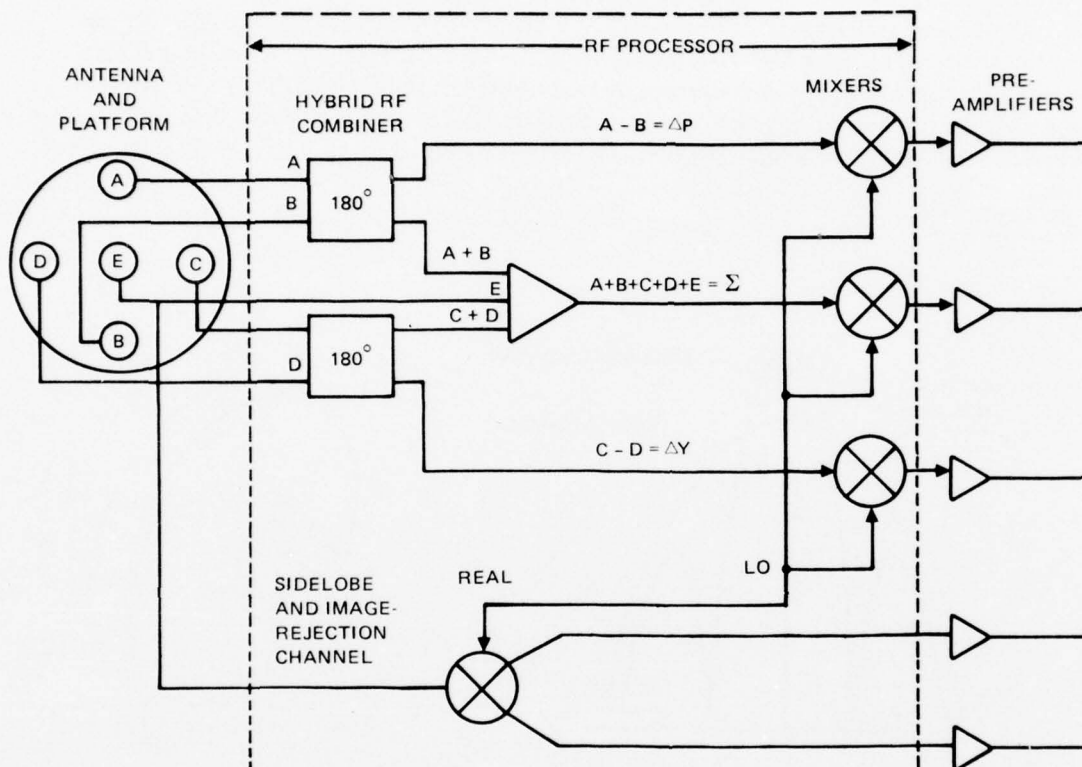


Figure 11. Rf assembly.

### SENSOR LOCAL OSCILLATOR

The local oscillator (LO) subsystem provides the LO signal to the antenna mixer assembly for frequency translation of the sum and difference signals to the intermediate frequency (IF). The local oscillator is a single YIG oscillator which covers all of the frequency bands of interest at BRATFAC.

### SENSOR IF PROCESSOR SUBSYSTEM

The IF processor subsystem (figure 12) includes preamplifiers and a narrowband IF receiver. A matched set of three preamplifiers is provided for the sum ( $\Sigma$ ) and the two difference ( $\Delta P$ ,  $\Delta Y$ ) channels: a matched pair is provided for the omni-real (OMR) and omni-image (OMNI) channels. The IF processor operates on the angle-tracking signals using a commutated phase-comparison, amplitude, monopulse technique. At the input to the receiver, the angle errors are proportional to the difference-channel amplitudes. At the



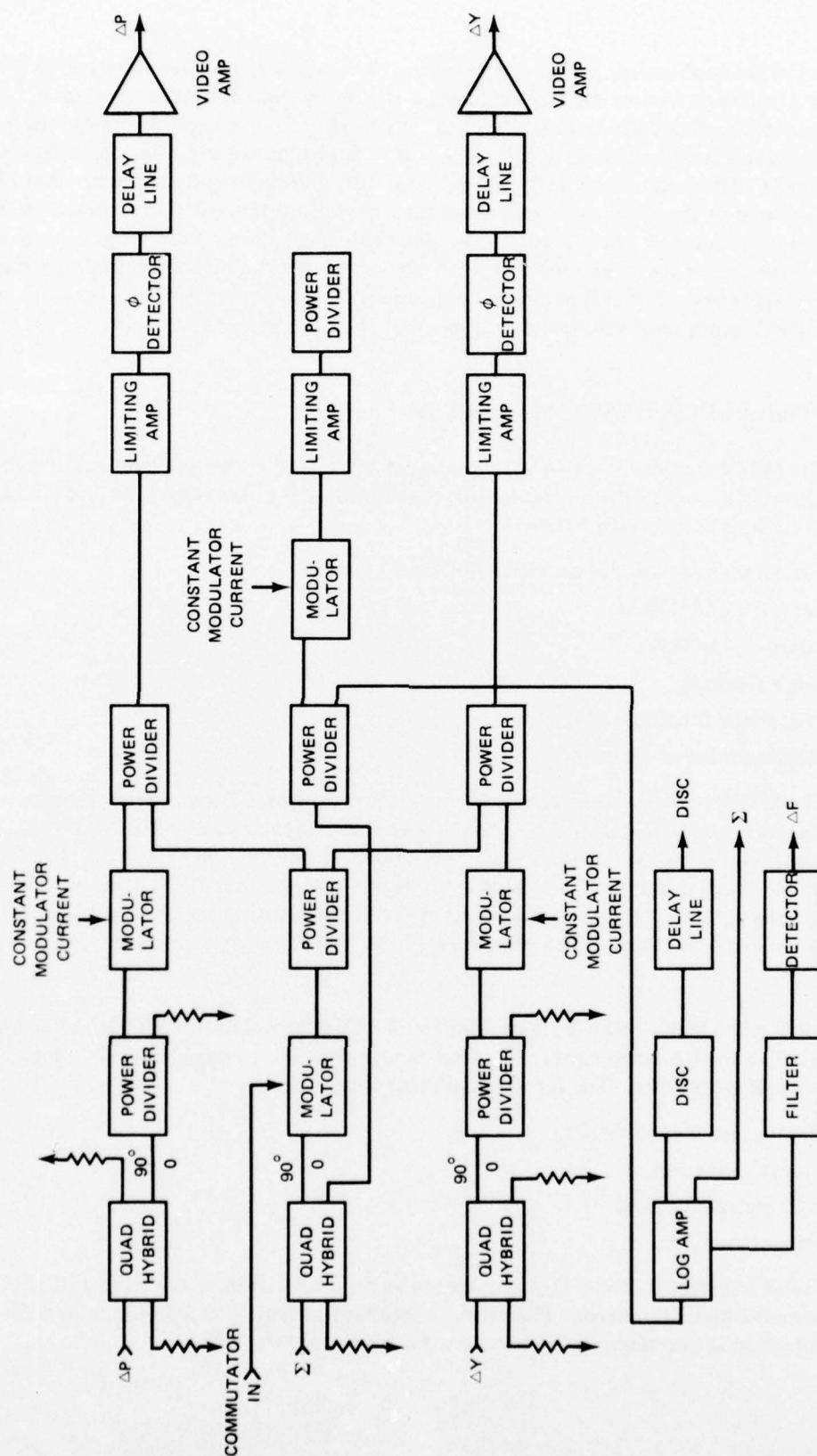


Figure 12. IF processor block diagram.



output at the preamplifier section of the receiver, the sum and the difference signals are added in a quadrature hybrid which transforms the difference-amplitude information into phase information. Since the error (difference) information is now represented by phase differences, signal amplitude is no longer critical and amplitude tracking and normalization is not required. The outputs of the hybrid are amplified and hard-limited. Determination of the magnitude of the difference errors, and the direction of the errors (up, down, or left and right) is accomplished in a phase-sensitive detector whose output amplitude is proportional to the cosine of the phase difference between the inputs and whose polarity defines direction of this error. The IF processor also produces outputs which are proportional to the log of the  $\Sigma$  input level and to the frequency of the  $\Sigma$  input signal.

#### MISSILE SEEKER DIGITAL PROCESSOR (MSDP)

The MSDP consists of a CDC-469 computer integrated with a pre- and post-processor (PAPP). It interfaces with the missile sensor, the autopilot, and the ARWS, and provides the BRAZO functions enumerated below:

- Signal conditioning and processing of sensor outputs,
- Frequency SEARCH,
- Parameter tracking,
- Angle tracking,
- Frequency tracking (AFC), and
- Missile guidance commands.

The MSDP receives video signals from the IF processor. These video inputs include monopulse pitch and yaw ( $\Delta P$  and  $\Delta Y$ ) to determine the angular position of the received target signal. The amplitude of the signal is determined from the sum video ( $\Sigma$ ). The frequency of the signal is derived from the output of the discriminator (DISC) and the coarse-frequency output ( $\Delta F$ ) is tested to determine if the signal is within the bandwidth of the discriminator's output filter. A block diagram of the MSDP is shown in figure 13.

**PRE- AND POST-PROCESSOR (PAPP) FUNCTIONAL DESCRIPTION.** The PAPP performs A/D and D/A conversions, the input/output signal processing, avionics interface, and the autopilot interface. The input signal processing includes:

- Analog signal conditioning,
- Target validation,
- A/D conversion, and
- Data storage.

The autopilot interface includes D/A conversion and amplification to drive the autopilot and the antenna platform servos. The avionics interface consists of a 100K-baud serial-parallel interface for message traffic between the ARWS and the MSDP.



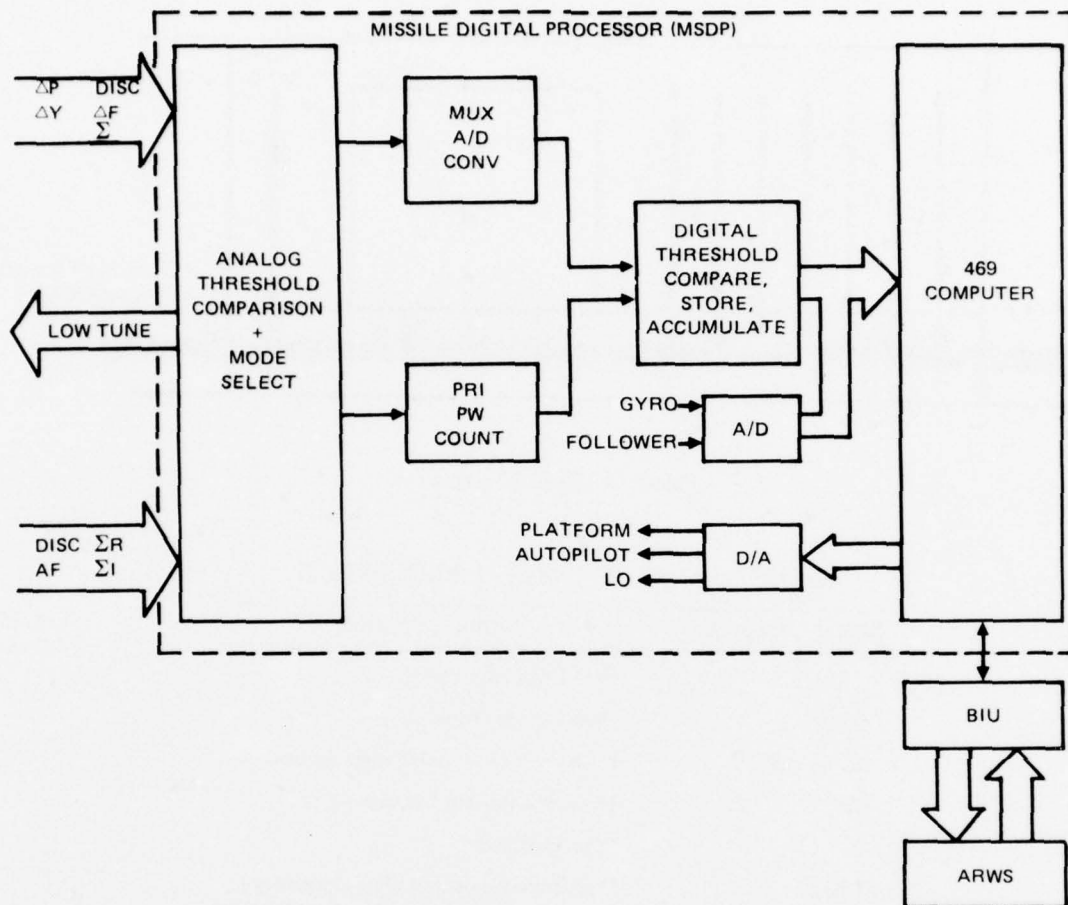


Figure 13. MSDP block diagram.

**PAPP HARDWARE DESCRIPTION.** The PAPP is made up of the following eight circuit boards located in the chassis as shown in figure 14 :

- Analog I,
- Analog II,
- Analog III,
- Timing and control,
- Counter logic,
- Arithmetic and logic unit (ALU),
- FIFO, and
- Test board.

The tests for correct frequency, amplitude, and main-lobe reception are performed on the Analog I board. The signals which are processed are shown in table 2.



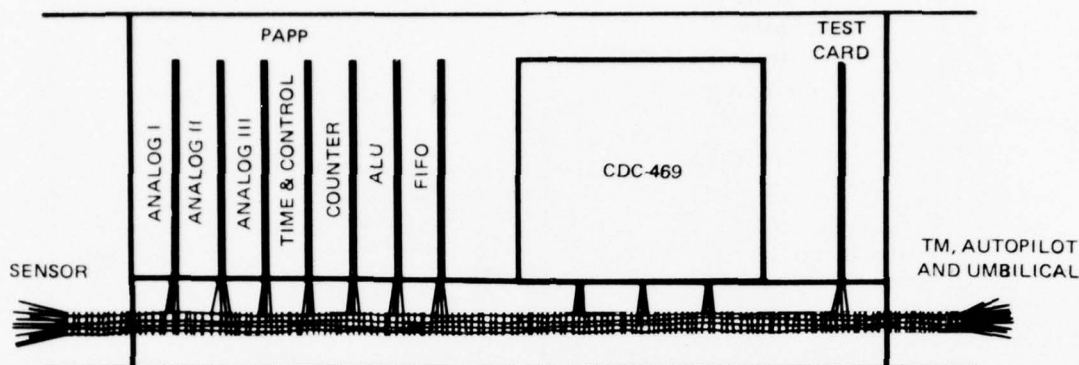


Figure 14. PAPP locations.

TABLE 2. ANALOG I SIGNAL PROCESSING.

Signal Designation	Name of Signal
$\Sigma\text{OMR}$	OMNI real amplitude,
$\Sigma\text{OMI}$	OMNI image amplitude,
$\Delta\text{PDF}, \Delta\text{YDF}$	Pitch, yaw monopulse angle signals,
$\Delta\text{F}$	IF output (coarse frequency),
$\Sigma$	Sum amplitude,
DISC	Discriminator output (fine frequency).

Receiver quantities  $\Delta\text{FDF}$  and  $\Sigma\text{DF}$  are compared against thresholds set by the CDC-469 computer to determine that the signal has the correct frequency and amplitude. The incoming pulse is tested by comparing the  $\Sigma\text{DF}$  signal with the  $\Sigma\text{OMR}$  signal. If  $\Sigma\text{DF} > \Sigma\text{OMI}$ , the signal is from the main lobe. The OMNI real signal is compared to the OMNI image for image rejection. If a pulse passes these tests, an A/D conversion cycle is initiated. Receiver quantities  $\Sigma$ ,  $\Delta\text{P}$ ,  $\Delta\text{Y}$ , and DISC (DF or OM) are digitized and held in a storage register for access by the ALU.

Analog II performs A/D conversion of servo inputs and serves as the solenoid drivers for the D/A converters of Analog III. The A/D conversion is controlled by the CDC-469 computer. One of the 4 servo input signals (P-gyro, Y-gyro, P-platform, Y-platform) is selected and a conversion cycle is initiated. The CDC-469 computer then accesses the digital data after allowing sufficient time for A/D conversion. The analog platform-drive signals from Analog III are amplified to drive the pitch and yaw hydraulic solenoids which position the antenna platform. The circuitry which performs this function was taken directly from the AIM-7. The analog inputs, P-OUT and Y-OUT, are amplified and drive the 4 solenoids P SOL 1, P SOL 2, Y SOL 1, and Y SOL 2.

Analog III contains the 6 D/A output channels. Each channel has a data register and a D/A converter. The CDC-469 computer addresses each channel by the designated channel



address and the D/A control bit. The digital data stored in the data register are converted to analog and proceed to Analog II for amplification.

The timing and control board produces all clock pulses, initialization timing, and control codes, and contains a program counter for the MSDP. For low-frequency clock pulses, a low-frequency clock is divided down to provide clocks which are multiples of 300 Hz. The high-frequency oscillator provides clock pulses of 20 MHz, 10 MHz, 4 MHz and 1 MHz. Initialization timing and the program counting are provided by a programmable counter. Combinations of the 2 counting cycles provide various timing signals. The control codes which specify all ALU operations and various control commands, are implemented by two 16-by-4 RAM, a 4-bit address counter, and a start/stop count flip-flop. The control codes are initially loaded from the CDC-469 computer.

The counter logic contains 3 sets of counters: PW counter, time-event counter, and the PRF counter and interrupt logic. The PW counter is an 8-bit binary counter counting the duration of the PW using a high-frequency clock. The output of the PW counter is strobed into the PW register and the 8 bits of the PW register are connected to the DF/OMR comparator output and used as a flag bit. The time-event counter counts at a lower frequency using a 16-bit counter. Time event is the amount of time between the leading edges of 2 consecutive valid pulses. The PRF counter and interrupt logic keep track of PRF ON and OFF and send an interrupt to the CDC-469 computer and the arithmetic and logic unit (ALU) at appropriate times. These interrupts are used in the ALU to initialize the integration process.

The arithmetic and logic unit (ALU) performs pulse validation and integration by successive approximations. The ALU first compares the four digital receiver inputs ( $\Delta P$ ,  $\Delta Y$ , PW, DISC) with thresholds set by the CDC-469 computer. If all pulse parameters are within the thresholds, integration of the receiver parameters begins. Extraneous targets are filtered from the integration cycle. The operations performed by the ALU are shown in table 3.

TABLE 3. ALU OPERATIONS.

$$\begin{aligned}\Sigma(\Sigma R) &\leftarrow \Sigma(\Sigma R) + \Sigma R, \\ \Sigma \Delta P &\leftarrow \Sigma \Delta P + \Delta P, \\ \Sigma \Delta Y &\leftarrow \Sigma \Delta Y + \Delta Y, \\ \Sigma PW &\leftarrow \Sigma PW + PW, \text{ and} \\ \Sigma DISC &\leftarrow \Sigma DISC + DISC.\end{aligned}$$

These partial sums are stored for access by the CDC-469 computer.

The first-in, first-out (FIFO) unit stores the digitized samples, R, P, Y, DISC, and the time-event count (TEC). It also provides the serial interface for the MSDP to the BRAVE. The digitized parameters from Analog I are each stored in a data channel. The FIFO output is an 8-bit word with 2 words being used for the TEC.

The eighth PAPP board, the test board, serves as the digital interface for the data-acquisition system and the CDC-469 computer. It contains differential line drivers and receivers for noise reduction over the cables to the test van.



**CDC-469 PROCESSOR.** The CDC-469 processor consists of a CDC-469 computer and its associated utility software. The computer is configured as a 16-bit, fractional two's-complement machine containing 8000 words of plated-wire memory. The computer has a 16-word, 16-bit register file, 4 levels of priority interrupt, and 3 address modes. The computer performs real-time target search, tracking, and target-identification algorithms using threat-file data from the ARWS and real-time pulse parameters accumulated in the PAPP. It controls the operation of the PAPP based upon the commands from ARWS and passes data to the ARWS for display. A description of the CDC-469 computer functions in the various modes is contained in Section 6.

#### ELECTRICAL CONVERSION UNIT

The electrical conversion unit (ECU) converts available power from the SPARROW electrical power unit (EPU) for use in the BRAZO seeker. Power from the EPU to the seeker includes  $\pm 100$  Vdc, 9 V at 1200 Hz, and +50 Vdc. The ECU converts this power to  $\pm 5$  Vdc,  $\pm 15$  Vdc, and -20 Vdc for use by the MSDP and the sensor. Minus 50 Vdc is generated in the ECU for use by the BRAZO seeker. Table 4 shows the AIM-7E and AIM-7 BRAZO power requirements.

TABLE 4. AIM-7E-2 AND AIM-7 BRAZO POWER REQUIREMENTS.

AIM-7E-2		BRAZO	
VOLTAGE	CURRENT (A)	VOLTAGE	CURRENT (A)
+28	(SQUIB FIRING)	+28	(SQUIB FIRING)
9 Vac, 1200 Hz, 2 phase	2.2 per phase	9 Vac, 1200 Hz, 2 phase	2.2 per phase
115 Vac, 400 Hz	(HEATER)	115 Vac, 400 Hz	(HEATER)
+25 Vdc	4.5	+25 Vdc	4.5
+50 Vdc	0.1	+50 Vdc	0.1
-100 Vdc	0.095	-100 Vdc	0.095
+100 Vdc	0.173	+100 Vdc	0.173
-280 Vdc	0.036	-20 Vdc	0.250
+255 Vdc	0.192	+15 Vdc	0.950
		-15 Vdc	1.1
		+5	7.6
		-5	0.2

#### TELEMETRY UNIT

The GTU-5 contains a modified AN/DKT-30 telemetry (TM) unit. A functional block diagram of the telemetry system is shown in figure 15. For BRATFAC testing, the summing network output will be connected directly by cable to the test van.



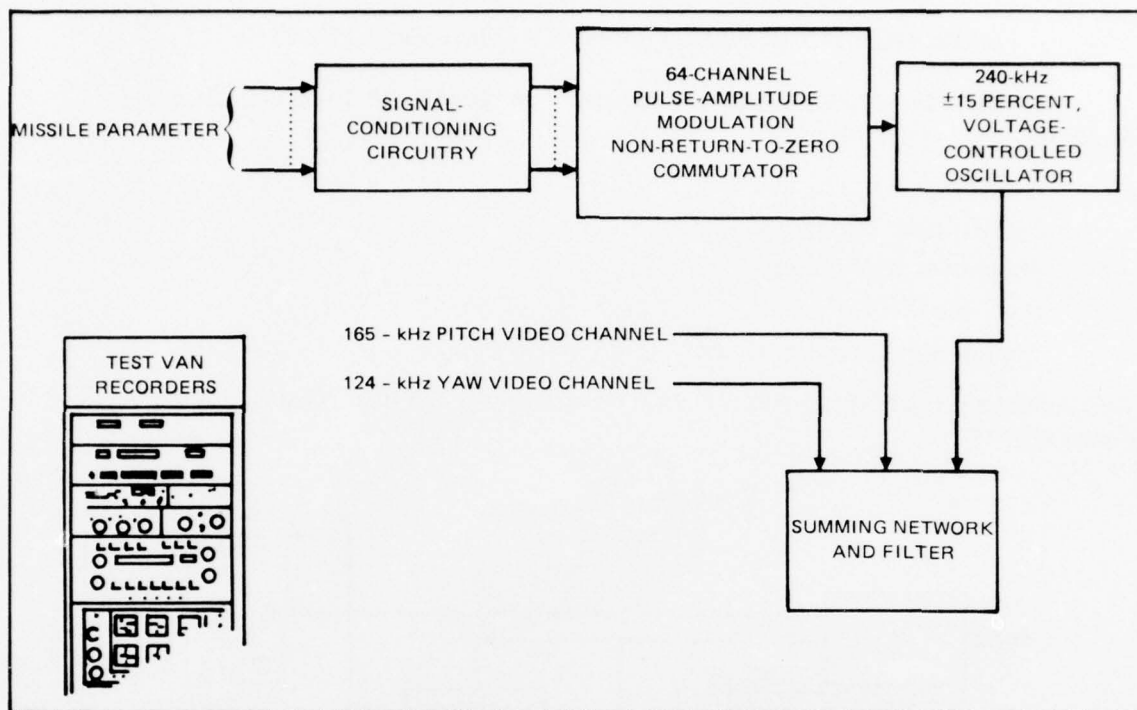


Figure 15. Modified SPARROW TM unit.



#### SECTION FOUR, BRAZO AVIONICS EQUIPMENT (BRAVE)

The BRAZO avionics equipment installed in the BRATFAC F-4B aircraft consists of the following major elements:

- ARWS radar-warning receiver,
- BRAZO interface module,
- Weapons-control system,
- Fire-control radar, and
- Aircraft displays and controls.

Relationships between the elements of the aircraft avionics and BRAZO are indicated in figure 16.

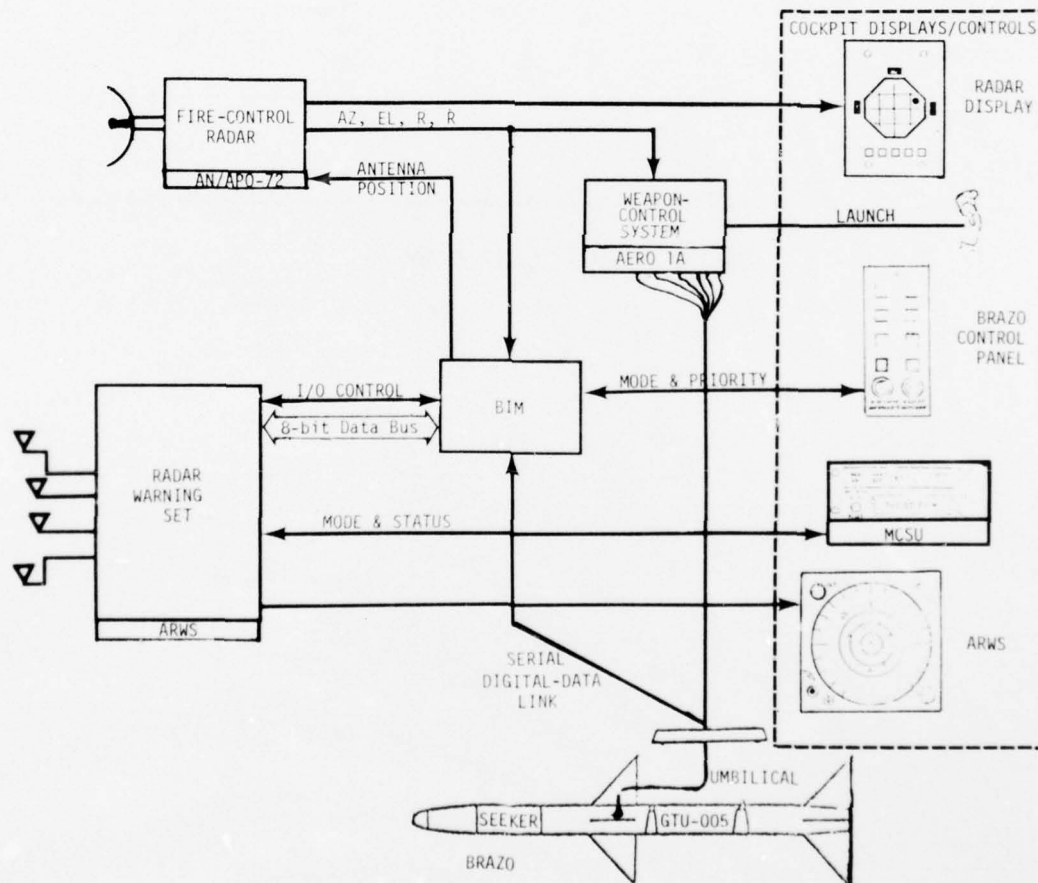


Figure 16. Avionics interface functional description.



## RADAR-WARNING RECEIVER

During BRATFAC testing, the advanced radar warning system (ARWS) is used as a stand-in radar-warning receiver (RWR). The ARWS is basically an AN/ALR-45 receiver set coupled to a digital processor (figure 17). The digital processor used in the ARWS is Applied Technology's Advanced Computer (ATAC). ARWS has two major functions: radar warning and BRAZO avionics processing.

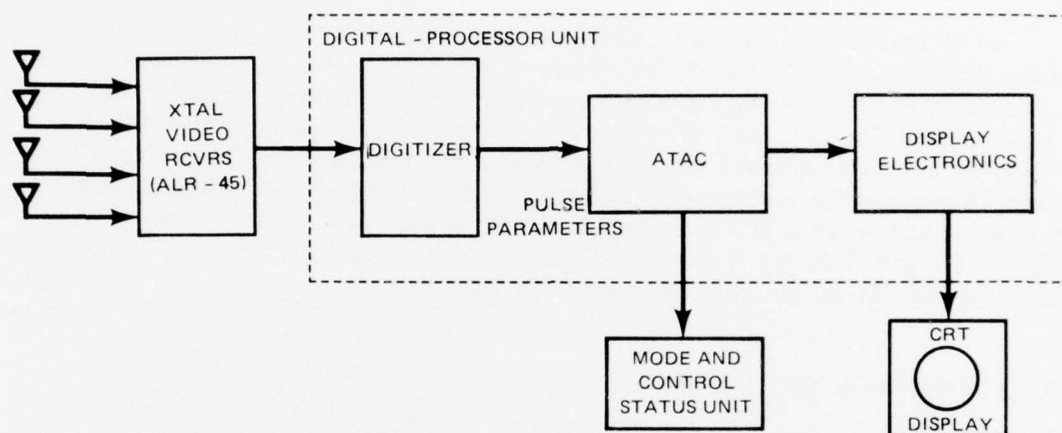


Figure 17. Radar-warning receiver.

## RADAR-WARNING FUNCTION

For radar warning, the ARWS uses an amplitude, monopulse, direction-finding (DF) system which utilizes four quadrant antennas, crystal-video receivers, and digital logic. The output of each antenna is passed to a 3-band crystal-video receiver, and the pulse outputs from these receivers are digitized and compared in the digital processor. The processor keeps track of the signals in all bands and provides input of azimuth and amplitude to a CRT within 2 seconds after its first detection. Threat characteristics and angular position are presented in the form of a stable, prioritized, alphanumeric display on the ARWS CRT. A rough approximation of range is made using the signal strength of the received signals and is displayed, PPI-style, on the bearing lines.

## BRAZO AVIONICS FUNCTIONS

Avionics processing for BRAZO is performed by a section of software in ATAC called the BRAVE Avionics Processor (BAP). BAP assembles and maintains the BRAZO system track file known as the Active Target Table (ATT), implements operator directives for system mode changes and target selection, and displays BRAZO-detected emitters on the ARWS display. Details of the BAP software are contained in Section 5.

The Test Van at BRATFAC contains a device which performs functions similar to those of BAP for the purpose of testing the BRAZO missile without having to use the



avionics on board the aircraft. This device is also referred to as BAP (BRAZO Avionics Processor). To distinguish between these two systems, the BRAVE Avionics Processor will be referred to as ATAC/BAP signifying the software implementation of BAP in the ATAC processor. The latter (BRAZO Avionics Processor), which is discussed in Section 6, will be referred to as the CDC/BAP.

### ATAC PROCESSOR

ATAC is a modular, compact, high-speed, digital processor which performs data-processing system control functions. ATAC utilizes a microprogrammed, wide-data-path micromemory. It is a 16-bit parallel, stored program, two's-complement computer with instructions which have a variable format and can directly address up to 65536 words of memory, with direct, immediate, relative and indexed addressing modes. The processor contains 16 general-purpose registers which may be used as accumulators or as index registers, thus eliminating much of the memory accessing required for single-accumulator machines. The processor allows up to 4 bidirectional direct memory access (DMA) channels which independently operate at a data rate of over 1.1 MHz.

### BRAZO INTERFACE MODULE (BIM)

The BRAZO Interface Module provides the required interface and format conversion between processors and other elements of the system. The interface block diagram is shown in figure 18.

The bulk of the interfacing between ARWS and the BRAZO system (MSDP, APQ-72, BCP) takes place via the link between the ARWS and the BIM with all information transfers controlled by ARWS. Information transfer from ARWS begins with the I/O demand signal which defines, for the BIM, the time during which data and commands from ARWS are valid and which strobes data into the interface registers. The BIM sends back an I/O acknowledge (I/O ACK) when the data have been received and the I/O demand is reset indicating the end of this particular data transaction.



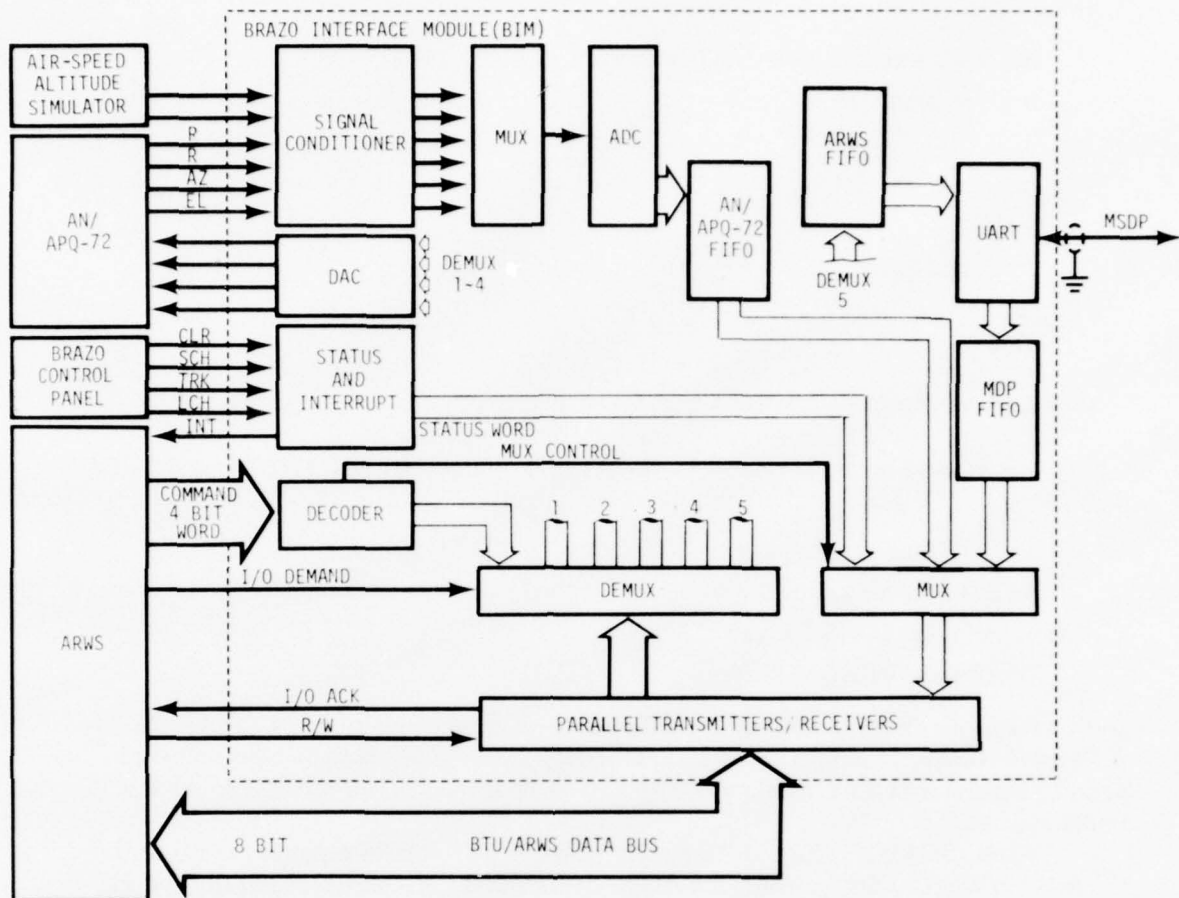


Figure 18. BRAZO interface module block diagram.

## ARWS-MSDP DATA EXCHANGES

Messages between the ARWS and MSDP are formatted into 8-bit bytes and 40-byte messages including 3 bytes of "overhead" for ID word, number of bytes following, and check-sum word. The contents and times of messages are determined by ARWS software. The threat-model table is sent in 40-byte messages. Thus, if 3.5 threat models were described in the first 40-byte message, the second 40-byte message would start with the middle of the fourth threat model. Link-error rate is controlled by the check-sum and acknowledge/not-acknowledge process. Overflows are ignored in the check-sum generation process. The hand-down track number and parameters message is also the TRACK command. When MSDP data arrive, a radar (AN/APQ-72) data demand occurs for AN/APQ-72 MSDP correlation.

Messages which can be transmitted between the ARWS and the MSDP are:

- Threat-model table,
- Frequency-control tables,
- Target parameters,



Hand-down track number and parameters,  
Position head,  
Gate set,  
ACK and NACK,  
Search,  
Track and launch, and  
Status.

#### ARWS - AN/APQ-72 DATA EXCHANGE

Messages which are to be sent between the ARWS and the AN/APQ-72 via the BIM include:

Az and El target position to ARWS,  
Az and El antenna positions,  
Target range to ARWS, and  
Target-range rate to ARWS.

If the data are to be sent to the APQ-72, the BIM will generate an interrupt for ARWS. ARWS will respond by sending BIM 2 bytes of information, each with a command word defining that information. Numbers 1 and 2 are given if the handoff target is an ARWS-found emitter.

When AN/APQ-72 data are to be sent to the ARWS, ARWS outputs an A/D convert bid to the BIM. The BIM converts the analog data from the AN/APQ-72, and fills the FIFO output buffer with the resulting data words, and interrupts ARWS. In response, ARWS reads these words in a predetermined order as follows: (1) azimuth, (2) elevation, (3) range, and (4) range rate.

#### ARWS-BRAZO CONTROL PANEL (BCP) DATA EXCHANGES

ARWS-to-BCP exchanges via the BIM deal with mode commands and status. Pushing a mode-command button on the BCP causes a BRAZO interrupt to be generated and sets one of bits 4 to 7 in the status word to ARWS. ARWS reads the status word and performs the indicated mode change. When this has been accomplished, ARWS sets one of bits 1 to 4 of its status word 2 and outputs this word to the BIM. The BIM, in turn, sets a MODE-status bit in its register which controls lights on the BCP, causing the appropriate mode-status indicator to light.

#### WEAPONS-CONTROL SYSTEM

The F-4B Aero-1A weapons control system consists of the following major groups of equipment: AN/APQ-72 radar set, cw transmitter, target-intercept computer, and missile-firing circuits. A functional block diagram of the AERO-1A MCS (less the missile-firing



circuits) is shown in figure 19. The AERO-1A has been modified to display the prioritized BRAZO targets, to acquire a designated target either manually or automatically, and to perform the initialization and computation necessary to launch.

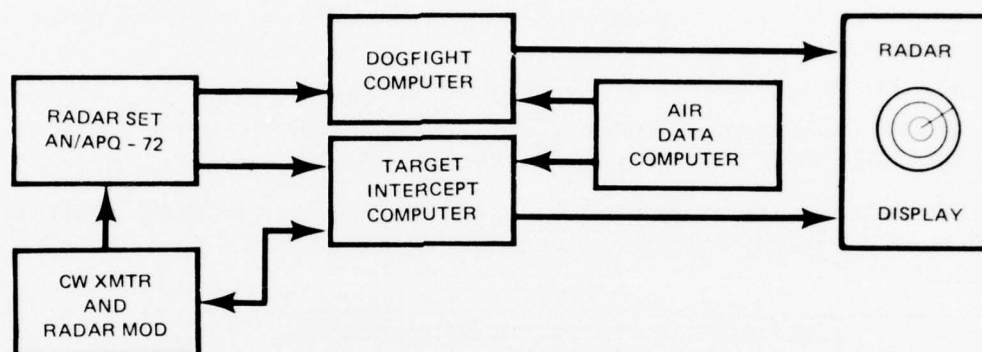


Figure 19. Functional AERO-1A block diagram.

## FIRE-CONTROL RADAR

The AN/APQ-72 fire-control radar provides a search and track capability. It is capable of range and angle tracking a target when lockon has been accomplished. A home-on-jam mode can be used if jamming is encountered while locked on. The AN/APQ-72 may be locked on the target by manual or automatic positioning of its acquisition symbol, and range-strobe position data can be generated in the BIM from BRAZO target data.

Once the AN/APQ-72 radar is locked on the target, it provides azimuth and elevation data to the ARWS for correlation with BRAZO data. If data correlation is correct, the operator is informed via display. If incorrect, the operator switches the AN/APQ-72 back to the acquisition mode and manually repositions to a new target. One output of the BRATFAC System tests will be to determine if automatic repositioning is possible. The AN/APQ-72 has been modified to provide antenna-position data, acquisition and range-strobe position data from an external source, and a lockon indication to the ARWS to initiate correlation processing.

## DISPLAYS AND CONTROLS

The BRATFAC test program utilizes existing weapons-system controls and displays. The AERO-1A weapon-control system (including the AN/APQ-72 radar) controls and displays are supplemented with a BRAZO Control Panel (BCP) and ARWS controls and displays, ie, mode control and status unit (MCSU) and the ARWS CRT.



## MODE CONTROL AND STATUS UNIT

The front panel of the MCSU is shown in figure 20. The search, track, and launch functions of BRAZO cannot be initiated until the BRAZO button on the MCSU is depressed. Pressing the BRAZO button after the ARWS is powered on and the BRAZO threat card has been substituted for the ARWS card, accomplishes 3 actions:

The BRAZO emitter library Threat-Model and Frequency-Control Tables are read into the ARWS and immediately transmitted to the MSDP and are not retained in ARWS RAM,

The BAP constants are read into ARWS RAM for later use, and

The BRAZO interrupt is enabled. Prior to pressing the BRAZO button, with the BRAZO MCSU PROM card in place, no BRAVE processing can take place.

The BIT (built-in test) light on the MCSU is activated for error modes in ARWS. A BIT error flag will be set if, after the ARWS attempts to send a message 10 times, 10 consecutive NAK's are received.



Figure 20. Mode control and status unit for BRAZO operation.

## ARWS DISPLAY

The ARWS CRT used to display detected emitters is shown in figure 21. Presentation of ARWS-detected emitters is limited to the single highest-priority threat. This emitter will always be marked with a diamond enhancement symbol. As many as 9 other emitters, all BRAZO targets, will be displayed. The highest-priority BRAZO target will be marked with a box enhancement symbol. The target so marked is the one which will be handed off to the BRAZO missile when TRACK mode is commanded from the BCP. The operator/pilot may change the marked target by switching to STEP on the MCSU. Each time this switch is pressed the next lower-priority target will be marked with the enhancement symbol. Switching to RESET will place the box back on the highest priority target. Pressing the PRIORITY button will cause the number of BRAZO targets displayed to be reduced from 9 to 4.



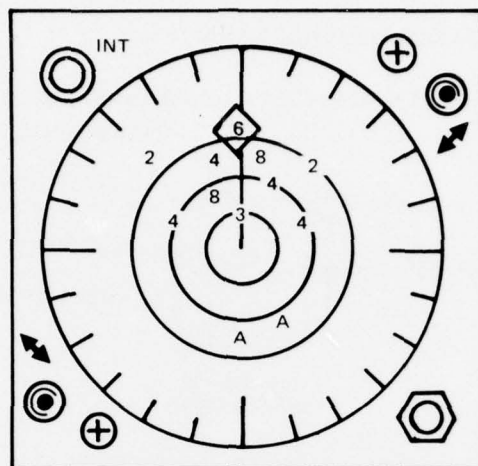


Figure 21. ARWS display.

#### BRAZO CONTROL PANEL (BCP)

The BCP (figure 22) enables the RIO to control all BRAZO operations during BRAT-FAC tests. Air-speed and altitude potentiometers on the BCP provide control of the air data simulator.

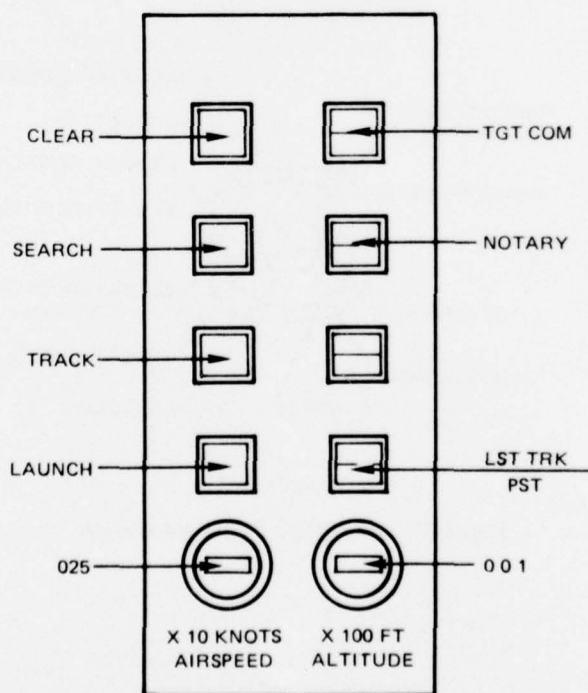


Figure 22. BRAZO control panel.



## AN/APQ-72 CONTROLS AND DISPLAYS

The symbology for the AN/APQ-72 search, acquisition and track modes is shown in figure 23.

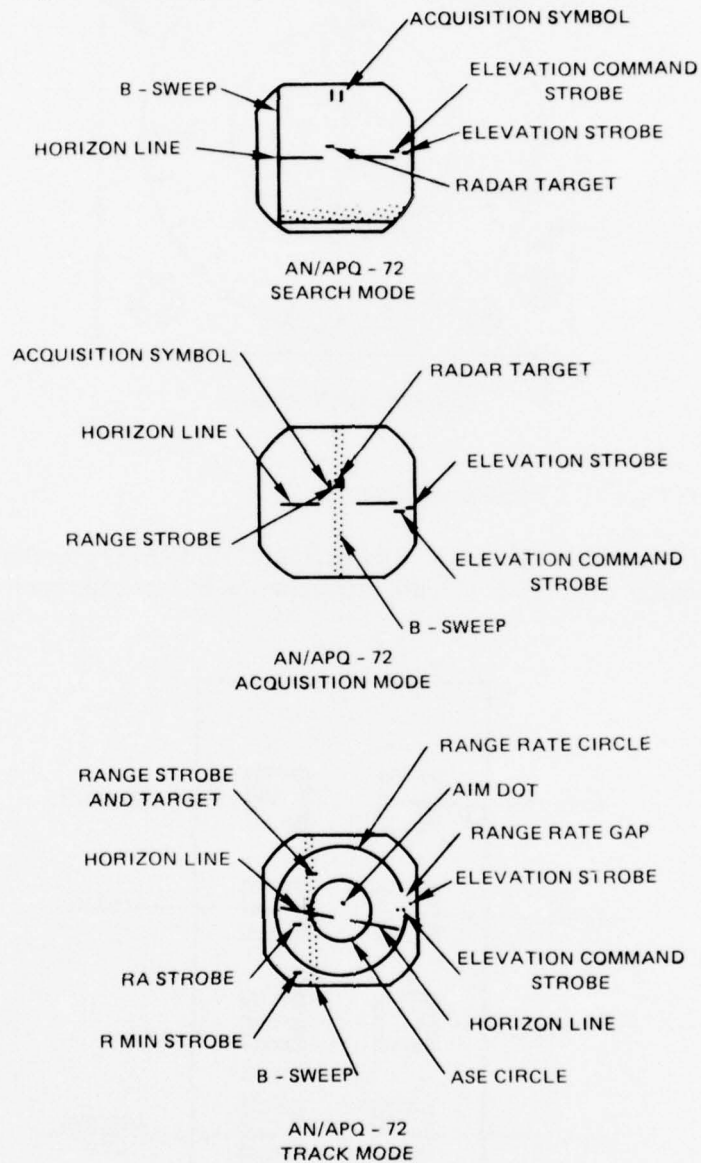


Figure 23. AN/APQ-72 display symbology.



## SECTION FIVE, SOFTWARE

The BRAZO system under test contains 2 main processors: the MSDP, which performs all of the BRAZO functions, and the ATAC, which performs the BRAVE functions. There are also 2 support processors at BRATFAC. A Texas Instruments-990 (TI990) system, located in the test van, performs data-acquisition and reduction functions. The Data-Acquisition System (DAS) is discussed in Section 6. Also located in the test van is an Intel-8080 system which simulates the BRAVE functions in order to allow operation of the MSDP without ARWS support. This processor is discussed in Section 6. The software which is resident in the CDC-469 (MSDP Software) and the ATAC (ARWS Software) is discussed in the following sections.

### MSDP SOFTWARE

The CDC-469 minicomputer in the MSDP performs 3 functions:

Searches for threat pulses and matches them with threat models  
(SEARCH Processor),

Performs pulse tracking, angle tracking and target lockon  
(TRACK Processor), and

Performs tracking to provide autopilot steering commands  
(LAUNCH Processor).

The BRAZO Supervisor routine oversees these MSDP software modules and calls other routines to handle commands from the BAP and from the PAPP. Commands from these external sources are received as interrupts. When an interrupt is received, control of the processing is transferred to the appropriate routine. This routine is determined by the level of interrupt. The lowest priority interrupt is the PAPP interrupt with the BAP interrupt second in priority. The highest priority interrupt is a clock interrupt. This interrupt comes from an external clock every 2 milliseconds and is used for timing.

### SEARCH PROCESSOR

The SEARCH Processor is responsible for surveying the threat-parameter space in the DF channel of the receiver for the presence of target pulses. Targets which are found by the SEARCH Processor are reported to the BAP for classification and further identification.

### TRACK PROCESSOR

The TRACK Processor is responsible for pulse tracking and target lockon. When the BAP commands the MSDP to track, the BRAZO track processor is called upon to find the target specified by the BAP. This is one of the targets found in the SEARCH mode and chosen by the operator for tracking. When the target is found, pulse tracking is performed to retain target lockon; then, angle tracking is performed. The parameters of the target are periodically reported to the BAP for correlation with AI radar data.



## LAUNCH PROCESSOR

The LAUNCH Processor tracks the target and provides steering commands to the Autopilot after launch. The same pulse-track and angle-track routines are used as in the TRACK Processor, pulse track is used for target lockon and angle track is used to drive the autopilot steering commands. When LAUNCH mode is entered, target parameters and time-to-impact are sent to the MSDP from the BAP. A set of countdown time and gain-value pairs is also handed down and used to update the steering gain to a specific value at specific times to provide finer autopilot control as the countdown time-to-impact approaches zero.

## ARWS SOFTWARE

### RWR PROCESSING

RWR processing includes:

- Threat characterization,
- Angular positions and range of threat, and
- ARWS display drive.

### BRAVE PROCESSING

BRAVE processing includes:

- Threat file sent to MSDP,
- Mode commands to MSDP determined and transferred,
- AN/APQ-72 and BRAZO target data correlated, and
- Active Target Table (ATT) maintained.

The software described in this section is the BRAVE software resident in ATAC. The ATAC/BAP program is a separate, interrupt-driven element in the ARWS program. When BRAVE processing is not being performed, RWR software controls the ARWS.

**CLEAR MODE.** As discussed in Section 2, BRAVE processing in the ARWS is initiated by a CLEAR mode command from the MCSU. This causes an interrupt which halts RWR processing and begins BRAVE processing.

**SEARCH MODE.** In SEARCH mode, the BAP's main function is to maintain and update the ATT, numbering the targets by priority. The ATAC/BAP commands the MSDP to begin search, then returns to normal RWR processing. When the MSDP sends back parameters on targets located, ATAC/BAP checks parameters against the ATT and assigns priorities to the targets. The highest priority targets (9 BRAZO and 1 RWR) are entered into the ATT



and displayed on the ARWS CRT. The remaining targets, and targets which are subsequently bumped from the table, are deleted from further processing. After each set of target parameters is displayed, control of the ARWS processing is returned to the Software Supervisor until another MSDP interrupt or mode change.

**TRACK MODE.** When TRACK mode is commanded, the ATAC/BAP sends a mode-change message to the MSDP, then searches the ATT and hands down the highest-priority target parameters to the MSDP. If the MSDP cannot find the target, a "not-found" message is sent to ATAC/BAP, and the process is repeated with the next highest-priority target. Each time the ATAC/BAP receives target parameters from the MSDP, it updates its target information for AN/APQ-72 correlation. If the ATAC/BAP receives a "lost-target" status from the MSDP and the lost target was tracked for less than 1 second, the next priority target will be sent to the MSDP for tracking. If a target was tracked for more than 1 second before being lost, the ATAC/BAP will dump the old ATT and return to SEARCH mode.

**LAUNCH MODE.** When LAUNCH mode is commanded, the time-to-impact and a track-loop gain versus time-to-impact table are computed by the ATAC/BAP. These data are sent to the MSDP along with a LAUNCH command. When angle lock is achieved by the MSDP, the operator will be informed via an indicator light on the BCP. When the missile is fired or angle lock is lost, ATAC/BAP automatically returns the system to CLEAR mode.



## SECTION SIX, INSTRUMENTATION VAN

The instrumentation van, dimensioned 8 feet by 20 feet\*, houses the test equipment, power sources, displays and controls, a test-conductor console, and work areas for up to 3 test persons. This van is shown in figure 24.

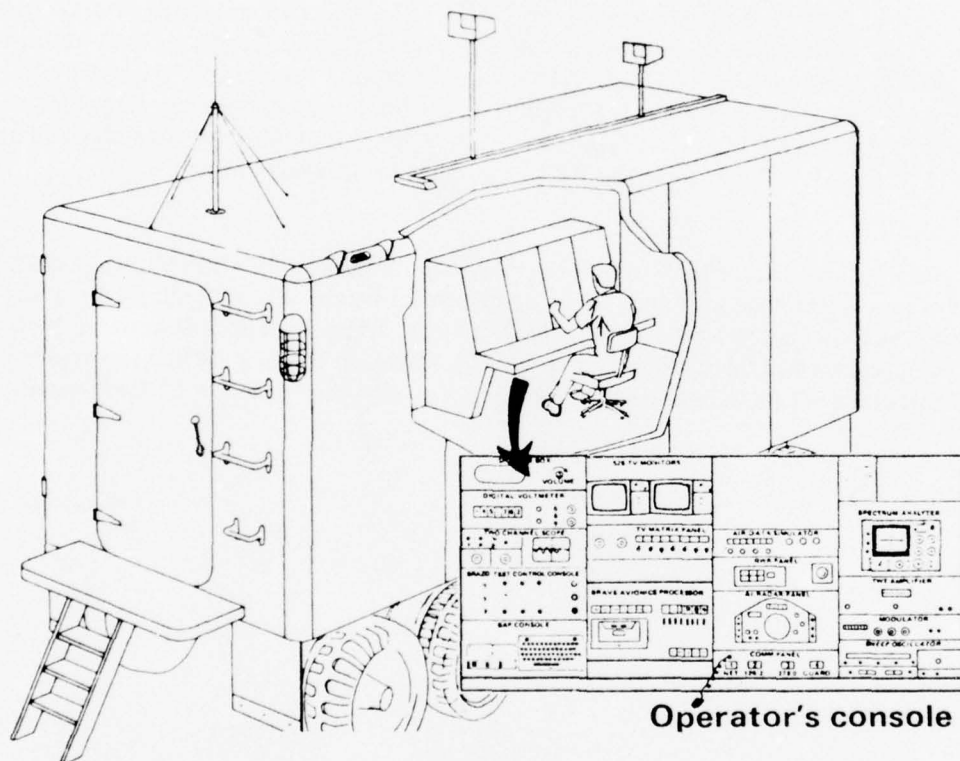


Figure 24. Instrumentation van.

The test-conductor console contains the instrumentation and controls required by the test conductor for monitoring and controlling the BRAZO test. Other test instrumentation, such as the data acquisition system (DAS), target simulators, jammers, timing equipment, TM recording equipment, and digital recording equipment, is contained in a set of instrumentation racks near the test-conductor console.

\*1 foot = approximately 0.3 metre.



## DATA-ACQUISITION SYSTEM (DAS)

The BRAZO missile system and associated avionics equipment are highly digitally oriented. Practically all weapon-system functions are controlled either by the RWR processor (ATAC) or the MSDP (CDC-469); consequently, digital-system parameters are conveniently available at I/O ports. The digital DAS monitors BRAZO system data transfers occurring at the B and D busses (ie, digital side of D/A and A/D converters) of the MSDP and on the parallel side of the BIM as well as reference instrumentation where test input parameters are available. The parameters which are monitored, time tagged, and recorded are summarized in table 5.

TABLE 5. DAS RECORDED PARAMETERS.

MONITORING POINT	DIGITAL DATA		
BIM	AN/APQ-72 TARGET DATA (AZ, EL, R, $\dot{R}$ , LOCK-ON)		A/D DATA (SIMULATED AIR-SPEED AND ALTITUDE)
	ARWS TO AN/APQ-72 DATA (AZ, EL, EST. R)		MDP TO ARWS MESSAGES ARWS TO MDP MESSAGES (EXCEPT TMT AND FCT)
B AND D BUSSES	MODE	INPUT (9 BUS)	OUTPUT (O BUS)
	SEARCH	FIFO A/D (DISCR, $\Sigma$ , $\Delta P$ , $\Delta Y$ , PW, TE)	LO TUNE
	TRACK/LAUNCH	SLOW A/D (P, Y-GYRO, AND PLAT-FORM FOLLOWUPS) ALU SUMS (VP, $\overline{VP}$ , $\Sigma R$ , $\Delta P$ , $\Delta Y$ , PW DISCR)	LO TUNE, PRF GATE P, Y PLATFORM DRIVE, P, Y ERROR ALU THRESHOLDS ( $\Delta P$ , $\Delta Y$ , PW, DISCR)
TCG	HH/MM/SS.XX		
MOUNT POSITION	12-BIT AZIMUTH ENCODER (0.1 DEGREE)		
TARGET SIMULATOR	FREQUENCY, PW, POWER LEVEL, SCAN RATE		
TACTICAL DATA SYSTEM (ASW-25)	INTERRUPT AZ, RANGE, ALTITUDE		

The BRATFAC data acquisition system (DAS) (figure 25) is built around a Texas Instruments 990/10 minicomputer with 32 K words of memory. Peripheral equipment includes:

- Video display terminal,
- Line printer,
- Cassette terminal,
- Disc drive, and
- 9-track tape drive.





Figure 25. Data-acquisition system.

A block diagram of the DAS with interfaces to other BRATFAC system components is shown in figure 26.



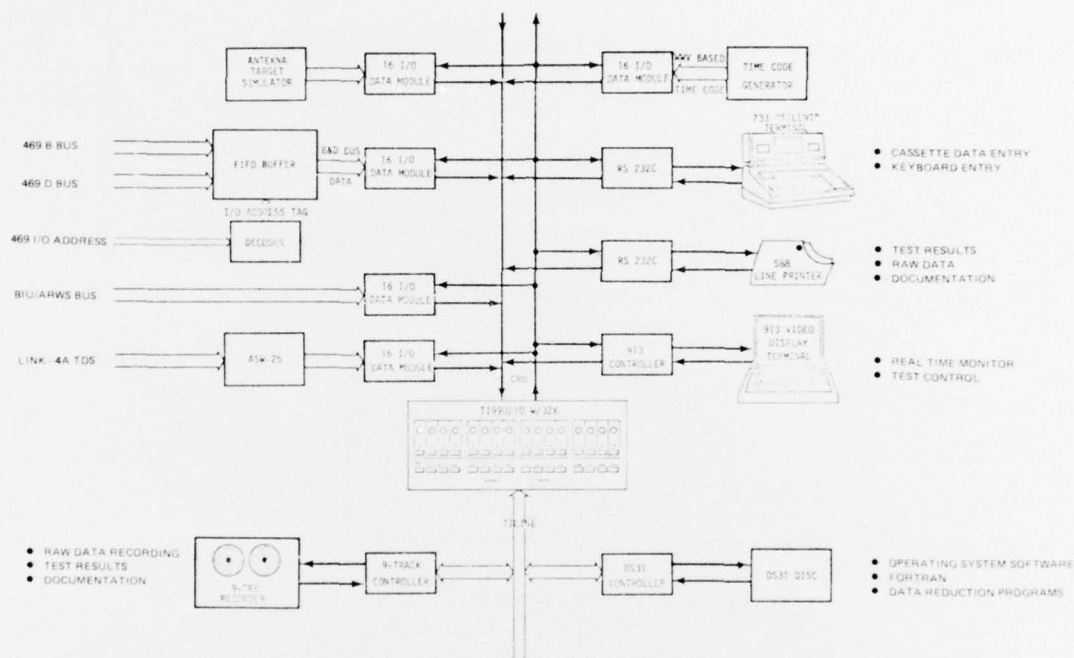


Figure 26. DAS block diagram.

The video display terminal acts as a real-time monitor of digital-system performance. Control of the DAS may also be handled by this terminal. Test results, raw-data listings, and documentation are printed on the line printer of the DAS. The 9-track tape drive and line printer combination provides raw-data recording, printout, and 2 separate means of recording test-data results and documentation. Raw data and test results on magnetic tape may be transported easily to other computer systems for further data analysis.

The disc drive houses a Fortran compiler and a software support library. Data-reduction software may also reside on disc or may enter the system via cassette tape or keyboard on the cassette terminal. This allows the data, recorded during a test day, to be reduced before the next day's tests. Output listings are then available for a "quick-look" analysis before proceeding with further testing. Interfacing with BRATFAC system elements is accomplished easily by standard TI-990 system interface components supplied by Texas Instruments.



## TARGET SIMULATOR

The BRATFAC target simulator consists of hardware which is built by Antekna, Inc. The major components of the system are:

Model 1418-11, multiple-scan pulse generator,  
Model 3400-05, fast-tuning source/modulator, and  
Model 7450, controller subsystem.

A simplified block diagram of the target simulator is shown in figure 27.

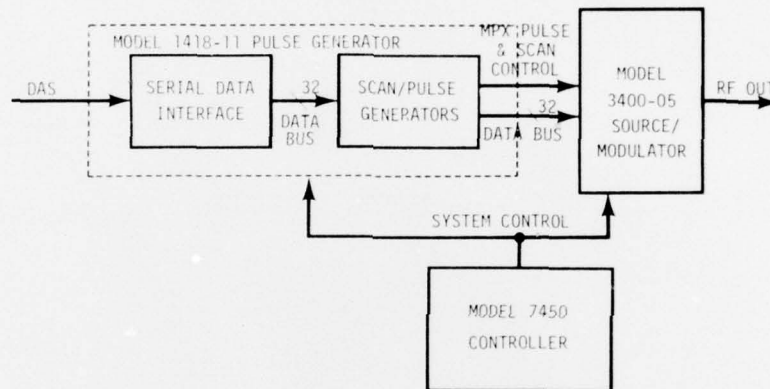


Figure 27. Target-simulator configuration.

The multiple-scan pulse generator generates scan and pulse patterns required to simulate simultaneously up to 16 pulsed emitters. It may be programmed by the DAS processor, using a standard RS-232C interface, to generate pulses with PRI of 0.5 to 6550  $\mu$ s and pulsewidths of 0.1 to 25.5  $\mu$ s. The following scan patterns may also be programmed using fixed or variable rates:

Circular,  
Track-while-scan,  
Conical,  
Sector,  
Raster,  
Spiral, and  
Palmer.

The following modulation modes are available:

PRI slide,  
Random pri,  
Multiple-position stagger,  
Pulse-burst group, and  
CW.



The source modulator generates up to 15 different frequencies and 15 different rf levels. These signals are modulated by the multiplexed scan-input signals and pulse trains from the pulse generator to simulate the pulsed emitters. The source/modulator and pulse generator are controlled by the controller subsystem to create a dense rf environment.

## JAMMING SIMULATORS

Three jamming simulators are available to BRATFAC to provide an ECM environment during selected portions of the test program. These are a noise generator, a serrodyne repeater, and the AN/DLQ-3.

### NOISE GENERATOR

The noise generator provides:

Continuous noise with a bandwidth of 5 MHz,

Blinking noise, 2 seconds ON, 2 seconds OFF, or 2 seconds ON, 1 second OFF,  
with 40-dB isolation,

Either manual or remote tuning, and

Adjustable power to 100 watts, effective radiated power.

### SERRODYNE REPEATER

*This repeater provides:*

Serrodyne from 0 to 120 kHz,

Deviation time from 4 to 16 seconds,

Input attenuation from 0 to 30 dB, and

Power of 20 watts.

### AN/DLQ-3

This equipment contains a BU-200 digitally programmed modulator and 9 pre-set, repetitive, pulse-repetition rate and duty-cycle programs.

### TIME-CODE GENERATOR

The DATUM Model 9150 time-code generator is the time standard for BRATFAC testing (figure 28). The significant components of this unit are described in the following paragraphs.



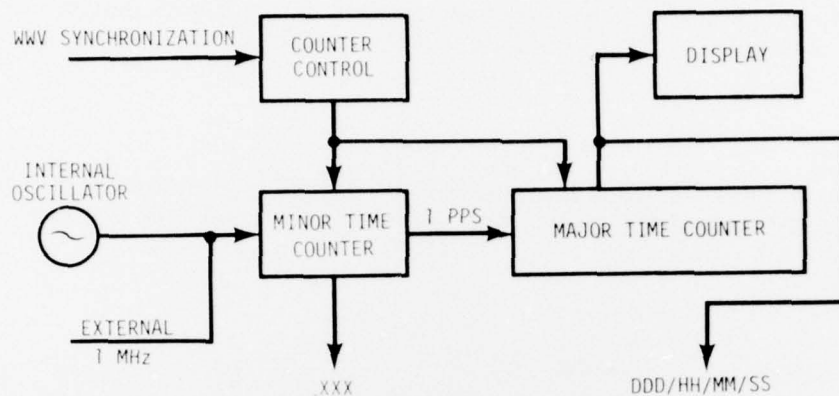


Figure 28. Time-code generator.

#### FREQUENCY SOURCE

The frequency source is a crystal-controlled oscillator or a 1-MHz external input.

#### MINOR TIME COUNTER

This unit (3 counters) divides the frequency of the source signal and develops the scan terms and rates required to develop serial time-code formats. This unit also supplies a 1-pps signal which is used to update the major time counter.

#### MAJOR TIME COUNTER

This counter stores the accumulated time count, usually in seconds, minutes, hours, and days. The accumulated count is the basis for the BCD parallel output supplied by the unit.

#### COUNTER CONTROL

The counter control is used to manually synchronize the major time counter and consists of switches to select and enter the time of day into the major time counter. Synchronization with radio station WWV is also available as an option and allows setting of the time-code generator to the broadcast time standard within an uncertainty of less than 2 milliseconds.

#### DISPLAY

This section receives data from the major time counter and provides an LED display of the accumulated time for the benefit of the user.



## PROGRAMMER CONSOLES

The programmer consoles provide for programming and debugging the computers. The CDC-469 programmer console and the separate video monitor will be used as a backup for the CDC-469 software checkout and the hardware maintenance when the BAP is not in operation. Figure 29 is a front view of the console and video monitor.

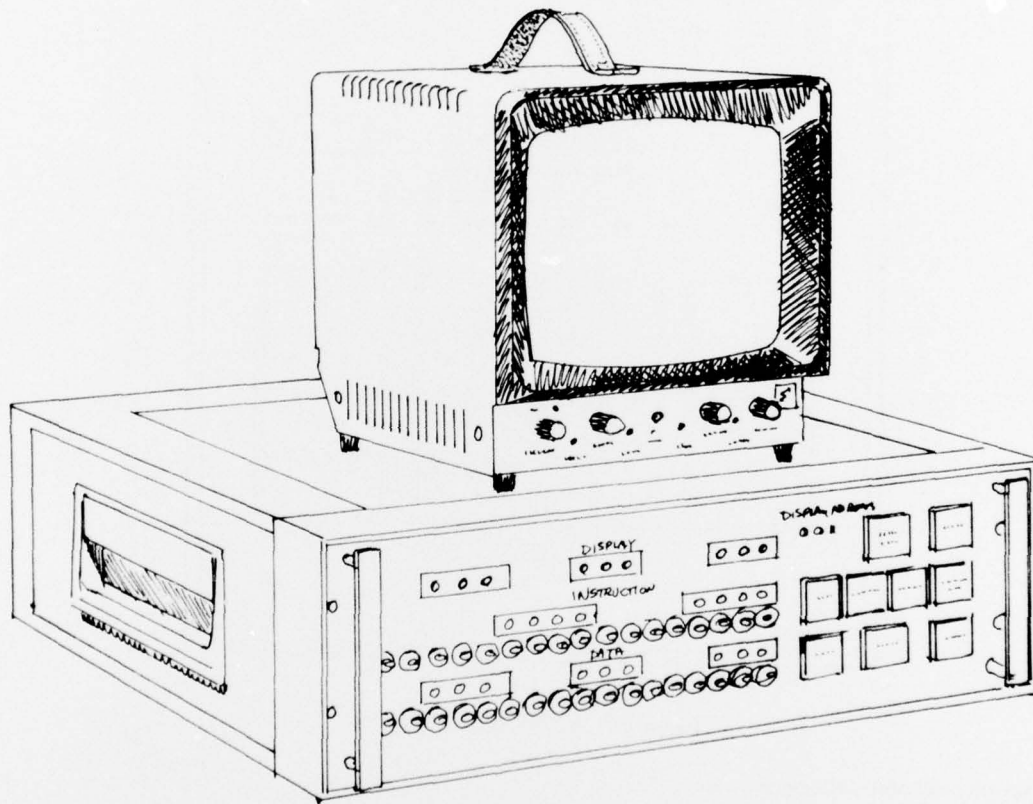


Figure 29. CDC-469 programmer console.

Control of ATAC for programming and debugging is provided by the ATAC-16 control panel (figure 30). This control panel allows the programmer to enter instructions in hexadecimal form into specified addresses in memory. The addresses and their contents are displayed on the panel. Control is also provided for entering the bootstrap loader into a specific area of memory and executing it to load a program from an external device such as a paper-tape reader. For debugging purposes, the contents of the various registers can be displayed as well as specific words in memory. Controls are also provided for loading the program counter and for executing the program a single step at a time.



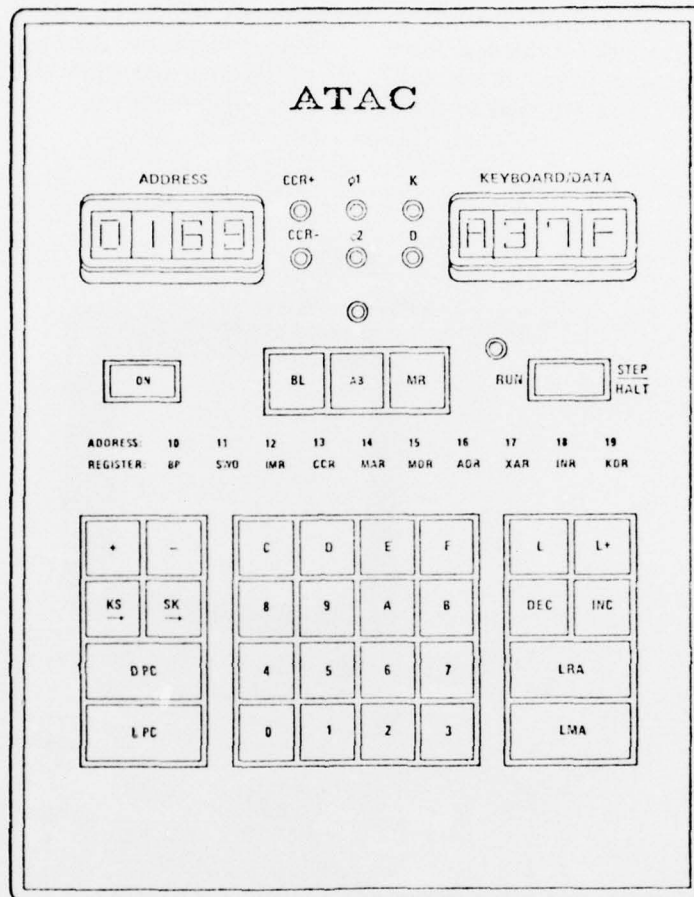


Figure 30. ATAC-16 control panel.

Examples of control entries are:

- Enter a hexadecimal value into the keyboard (KB) register,
- Inspect or change contents of a ATAC memory address,
- Enter 10 consecutive memory locations with a constant,
- Inspect or change contents of general or special registers,
- Execute one (or more) single ATAC instruction(s),
- Run an ATAC program.



## BRAZO AVIONICS PROCESSOR

The purpose of the CDC BRAZO Avionics Processor (CDC/BAP) is to complete the digital communication link for the MSDP, provide the necessary data in the proper format for controlling the MSDP, and to provide a means of receiving, processing, and displaying the digital data transmitted from the MSDP. The CDC/BAP (figure 31) was intended for use only in the initial laboratory checkout and testing of the MDP. During on-site system testing and evaluation, it will be replaced by the ATAC/BAP incorporated into the radar-warning receiver (RWR). However, the CDC/BAP will be available on-site as a back-up for the ATAC/BAP so that independent tests may be conducted on the BRAZO seeker.

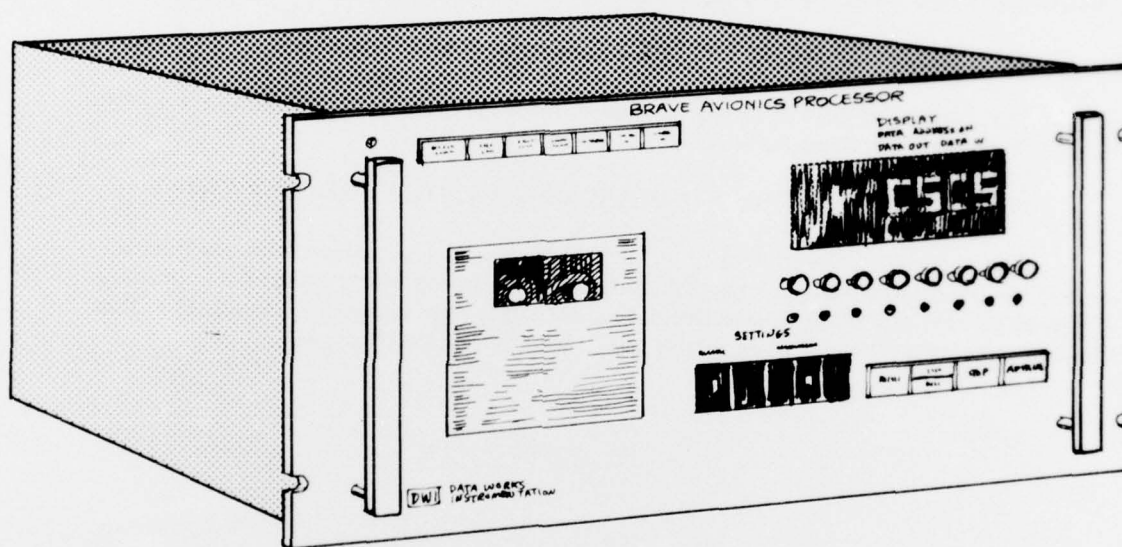


Figure 31. CDC-BRAZO avionics processor.

The CDC/BAP consists of a microprocessor (Intel 8080), a magnetic-tape cassette drive, a Teletype (TTY), and a cathode-ray tube (CRT) display and keyboard. The functions of the CDC/BAP include:

### DISPLAY OF DATA RECEIVED FROM THE MSDP

The purpose of the display function is to provide the operator with visual results of the MSDP operation. Also included are the location of corresponding data in the data base, converting the data from binary to digital form, and decoding and displaying error messages and MSDP status messages. The CRT is used for this function.



#### PROCESSING OF MSDP COMMANDS ENTERED BY THE OPERATOR

The purpose of the command function is to collect the appropriate data from the data base, format them into the proper MSDP message, and transmit the message to the MSDP. This function also verifies that the MSDP has received the message correctly. The CRT keyboard is used for this purpose.

#### STORAGE OF DATA TABLES ON THE MAGNETIC TAPE

The purpose of the data storage is to store, on magnetic tape, the data tables which the MSDP requires for its operation. Control of the magnetic tape is from the operator commands entered from the CRT keyboard.

#### RETRIEVAL OF DATA TABLES FROM THE MAGNETIC TAPE

The purpose of data retrieval is to build, from magnetic tape, the data tables which the MSDP requires for its operation.

#### PROCESSING CONTROL COMMANDS ENTERED BY THE OPERATOR

The purpose of the control function is to display the operator's keyboard entry, decode the entry, and transfer program control to the appropriate routines for processing. Although all entries are in the same format, some of the entries control operations within the BAP simulator whereas other entries control the operation of the MSDP.



## SECTION SEVEN, TEST-SITE FACILITIES

### F-4B TEST BED

An F-4B aircraft has been mounted on a 5-inch gun turret for use as a test bed for BRAZO (figure 32). The mount provides the capability to train the aircraft in azimuth with line-of-sight to the Pacific Missile Range and the Air Combat Maneuvering Range (ACMR) at Yuma, Arizona (figure 33). A governor controls the slew rate at 2 different speeds: 10 degrees per second and 30 degrees per second. The elevation angle is fixed at approximately zero degrees. A 15-degree positional dead zone will be initially centered at a compass heading of 45 degrees.

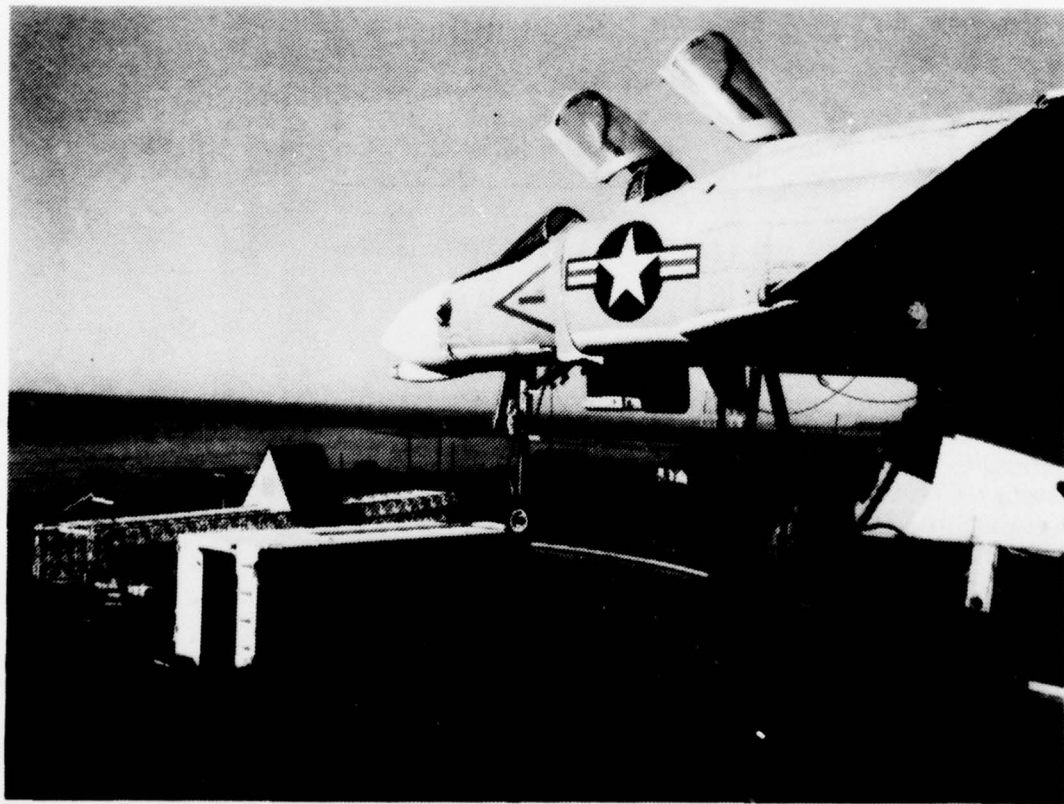


Figure 32. F-4B at BRATFAC.



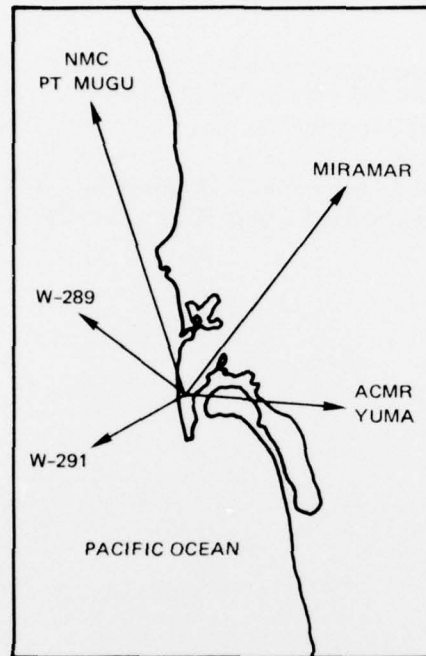


Figure 33. Centralized BRATFAC location.

#### F-4B MODIFICATIONS

The F-4B has been modified to permit the carriage of BRAZO missile at the right inboard external store station. The modification includes the installation of a BRAZO control panel in the rear cockpit, installation of a modified LAU-17/A missile pylon at the existing right inboard pylon-attachment hard points, and changes to existing internal wiring to provide BRAZO missile control, BRAZO instrumentation signals, and AIM 7E-2 missile-firing circuits routed through the existing aircraft pylon disconnects to the modified LAU-17/A missile pylon (figure 34).



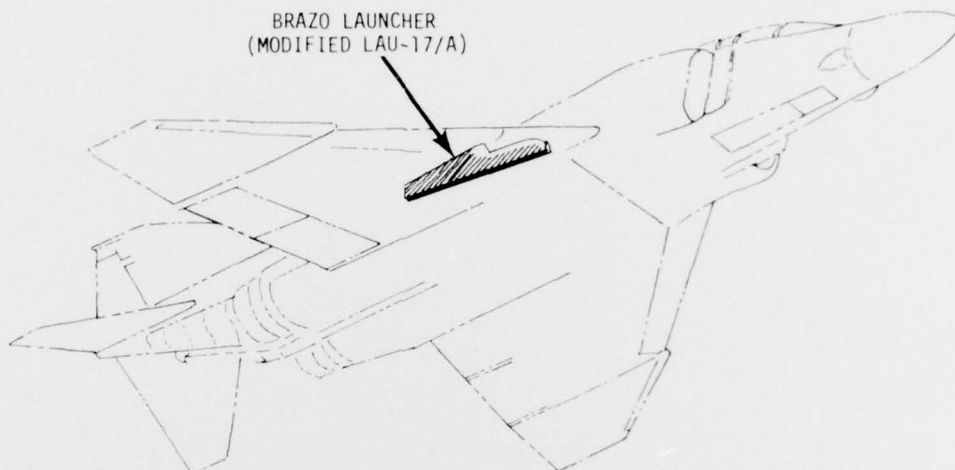


Figure 34. BRAZO modification.

Space for the BRAZO Control Panel has been provided by removing the Labs Release Angle control panel and the adjacent blank panel from the rear cockpit right instrument subpanel.

The LAU-17/A missile pylon modifications consist of repackaging the existing TG-76/ APA-128 tuning drive unit to house BRAZO electronic control components, and rewiring the pylon to provide BRAZO missile control and firing circuits through connectors matching the existing F-4B inboard pylon disconnects.

## COMMUNICATIONS

A communication network is provided between the test van, F-4B aircraft, and data-storage area for test-activity coordination. A uhf/vhf transmitter-receiver is also available for communication with aircrews undergoing ACM training with those in dedicated aircraft.



## APPENDIX A: GLOSSARY

ACM	Air Combat Maneuvering
ADM	Advanced Development Missile
AI	Airborne Interceptor
ALU	Arithmetic and Logic Unit
ARH	Anti-Radiation Homing
ARM	Anti-Radiation Missile
ARWS	Advanced Radar Warning System
ATAC	Applied Technology's Advanced Computer
ATAC/BAP	BRAVE Avionics Processor implemented in ATAC
ATT	Active Target Table
BCP	BRAZO Control Panel
BIM	BRAZO Interface Module
BRATFAC	BRAZO Avionics Test Facility
BRAVE	BRAZO Avionics Equipment
BRAZO	Spanish word for Arm (acronym for Anti-Radiation Missile)
CDC/BAP	BRAZO Avionics Processor implemented by CDC
CPU	Central Processing Unit
CRT	Cathode Ray Tube
CW	Continuous Wave
DAS	Data Acquisition System
DF	Direction Finding
DMA	Direct Memory Access
ECU	Electrical Conversion Unit
ERASE	Electromagnetic Radiation Source Elimination
FIFO	First-in-First-out
GTU	Guidance Test Unit
IF	Intermediate Frequency
I/O	Input/Output
LO	Local Oscillator
MCS	Missile Control System
MCSU	Mode Control and Status Unit
MSDP	Missile Seeker Digital Processor
NELC	Naval Electronics Laboratory Center



OMNI	Omnidirectional
PAPP	Pre-and-Post Processor
PRI	Pulse Repetition Interval
PRF	Pulse Repetition Frequency
RWR	Radar Warning Receiver
TM	Telemetry
UART	Universal Asynchronous Receiver Transmitter
WCS	Weapon Control System
YIG	Yittrium Iron Garnet



**APPENDIX B:  
BIBLIOGRAPHY**

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